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MIDS NETWORK CONTROL AND DIGITAL DATA SUBSYSTEM DESIGNS

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REVIEW AND APPROVAL

During 1972-73 a Base Communications Mission Analysis (BCMA) was conducted at ESD to examine requirements and options for improving and/or replacing Air Force base level communications systems. Several alternatives in two main categories were identified: (1) to optimize wire-pair/switched systems in current use or (2) use a coaxial cable system to provide a "bus" multimode transmission facility in which channelization is achieved by frequency/time division multiplexing techniques rather than by switched wire pairs.

The BCMA concluded that the second alternative would be more economical on a life cycle basis for the anticipated increase in "desk top" workstation data terminals. As a result, a follow-on project called the Air Force Base Information Transfer System (AFBITS) was undertaken at ESD to examine the multimode system alternatives in greater technical detail. This is the terminal report of the MITRE technical support to the AFBITS project.

Since the concept is applicable to many types of communication complexes, commercial as well as military, the title "Multimode Information Distribution System" (MIDS) is more descriptive of the design concept set forth in this report.

This technical report has been reviewed and is approved for publication.

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COAXIAL CABLE DATA DISTRIBUTION
INTERACTIVE TERMINALS
MICROPROCESSOR APPLICATIONS
MULTIMODE INFORMATION DISTRIBUTION
SIGNALING AND SUPERVISION

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The Multimode Information Distribution System (MIDS) is a local area telecommunications system capable of simultaneously handling digital data, video and voice traffic for a multitude of subscribers in a variety of connectivity patterns on wideband media such as coaxial cable. The designs for a MIDS data distribution subsystem and a multimode network control subsystem based on time division multiplexed techniques

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20. ABSTRACT

are described. The use of a novel, adaptive data rate feature provides high-speed service to any terminal as required without dedicating excessive amounts of capacity to particular terminals. These designs are oriented toward maximum use of current microprocessor technology.

FOREWORD

The system and subsystem designs for a local area multimode information distribution system described in this report have been developed in response to needs for improved and modernized telecommunications on military bases. This design for a common-user communication system is based on the multiplex-bus architecture. The numbers of subscribers, data rates and specific design techniques described have been selected solely for the purpose of conducting a technical feasibility demonstration and do not necessarily represent the service parameters and techniques that would be applicable for an operational system design.

The purpose of the technical feasibility demonstration is to provide sufficient technical data to assess the technical risks of an operational implementation, to provide cost factors for life cycle costing and to establish technical parameters for preparing system specifications.

This project was performed by The MITRE Corporation under sponsorship of the Electronic Systems Division, Air Force Systems Command.

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GLOSSARY OF ABBREVIATIONS AND ACRONYMS

ACC	Accumulator
ADR	Asynchronous Data Receiver
ASCII	American Standard Code for Information Interchange
bps	bits per second
CATV	Community Antenna Television
CCIS	Common Channel Interoffice Signaling
CCITT	Consultative Committee of International Telegraph and Telephone
CPU	Central Processing Unit
CVSD	Continuous Variable Slope Delta
dbmv	decibels with respect to 1 millivolt (0 dbmv=1mv)
DMA	Direct Memory Access
EBCDIC	Extended binary Coded Decimal Interchange Code
EPROM	Erasable and Programmable Read Only Memory
FDM	Frequency Division Multiplex
FIFO	First-in First-out
IIL	Integrated Injection Logic
IR&D	Independent Research and Development
KBD	Keyboard
kbps	kilobits per second
LSI	Large Scale Integrated
MIDS	Multimode Information Distribution System
MOS	Metal-oxide semiconductor
mv	millivolt
PACE	Processing and Control Element
PFEP	Programmed Front-End Processor
PROM	Programmable Read Only Memory
RAM	Random Access Memory
RF	Radio Frequency
RMS	Root Mean Square
ROM	Read Only Memory
S&S	Signaling and Supervision
TDM	Time Division Multiplex
TPM	Tri-Phase Modulation
TTL	Transistor-transistor logic
UART	Universal Asynchronous Receiver Transmitter

SECTION I

INTRODUCTION

1.1 BACKGROUND

The communications facilities that interconnect the various sensors and information processors are an important element of Command and Control systems. These communications facilities must be capable of handling a wide variety of analog and digital signals for voice, data and video traffic. During the last few decades substantial improvements have been made in the capabilities of long haul wideband trunk communications systems by employing microwave and troposcatter radio links and communications satellite links. For local signal distribution on an air base, within a local operating area or in command center complexes, communications were handled primarily by means of individual pairs of wires, cables or radio links interconnecting each user or equipment. Flexibility of interconnection is provided by means of patch panels and/or electromechanical circuit switches.

Recent advances in digital technology and broadband transmission media now permit the development of Multimode Information Distribution Systems (MIDS) employing "multiplex bus" techniques for local distribution communications. Multiplex refers to combining many different signals on a single transmission system. This technique is commonly used for long haul communications. The term "bus" indicates the capability to serve a number of geographically distributed terminals in a local area. These multiplex bus systems offer improved performance, versatility and portability at less cost, bulk and weight than current local distribution communications facilities.

Broadband communications over coaxial cable and through optic fibers are now state-of-the-art. Technological advances in digital technology permit the implementation of low cost frequency division and time division multiple access to a broadband bus. A variety of communication services then becomes possible for many users. Command and control communications in the future should be capable of handling multi-megabit data rates and multi-channel secure telephone and video transmission. The presentation of remote radar and other surveillance signals, as well as the standard visual display terminal information, will be accomodated. The technical capability of accomplishing these multiple services under a single communication control utilizing a single transmission medium will permit the dynamic reallocation of communication resources in accordance with demand.

1.2 OPERATIONAL ASPECTS

A multimode communications system will provide the connection between a user's terminal and information sources such as minicomputers, large host processors, microfiche storage, and other data, video and audio information sources. For example, a user visual display terminal may be used as a monitor for a surveillance or command situation and may also be used for entering text into a word processing system for preparation of messages, status reports and correspondence. The same terminal may also be used to query an information bank in a host processor or it may be connected into a distributed-processing system consisting of minicomputers with each having a specialized processing function. Since the digital data distribution and control subsystems occupy only two channels of the multi-channel coaxial cable, many other uses of the cable are simultaneously possible as described in References 1 and 2.

The principal technical capability required for the implementation of a multimode information distribution system is a supervision and signaling subsystem to control connectivity and a digital data distribution subsystem for data transfer. The experimental work to date therefore as described in this report has been specifically addressed to the data interconnection and control aspects of a MIDS using coaxial cable as the transmission medium.

1.3 DATA SYSTEM TRAFFIC CHARACTERISTICS

Data traffic is a function of the transmission rate of the subscribers' terminals and the number of subscribers requesting simultaneous use of the service. Terminal transmission rates can vary from as low as 110 bits per second for electromechanical printers to tens of kilobits/sec for visual display terminals. The number of user terminals performing transactions simultaneously can vary from a low value in slack periods to a high value during peak activity periods. Not all terminals however need the capability for simultaneous transmission or reception. For example, if a visual display terminal is supplied with one or more pages of storage, the terminal operator may begin entering data into the terminal's storage without actually transmitting any information to another computer or terminal. After entering a page of information, many terminals allow the operator to make text-editing changes, again without transmitting to a central computer. When the terminal operator has entered the information correctly, the entire screen of information needs to be transferred at high speed to its destination. The requirement, then, is for a system capable of handling bursts of information at high speed for short periods of times.

The MIDS design accommodates this requirement by providing a standard low speed of 600 bps capable of automatically switching to 19.2 kbps in accordance with the transmission requirements of the individual terminals. The dynamic switching is automatic and does not require any user action. Since only a small number of users are actually transmitting at any one time, the overall system transmission rate may be kept to a reasonable upper value.

SECTION II

MIDS SYSTEM DESCRIPTION

2.1 GENERAL

A Multimode Information Distribution System (MIDS) is a telecommunications facility capable of simultaneously handling digital data, video and voice traffic multiplexed on a single transmission system that serves a multitude of geographically distributed subscribers. For local information distribution in areas ranging in size from a command center complex or shelter to an airbase or similar size operational area, broadband coaxial cable of the type extensively used by the CATV industry is currently the most economical transmission media. Future developments in fiber optics will also be applicable for MIDS transmission links.

A MIDS must be able to provide a variety of connectivities including:

- o Point-to-Point (terminal-to-terminal/person-to-person)
- o One-to-many (multipoint or broadcast)
- o Many-to-one (remote terminals to Automatic Data Processing computer)

2.2 INFORMATION TRANSFER SERVICES

The information transfer services possible with a MIDS may be provided by using an integrated set of subsystems. Pertinent characteristics of each subsystem are described in the following subsections.

2.2.1 Common Channel Network Control Subsystem

The network control subsystem for a MIDS is provided by a separate out-of-band, polled, asynchronous, time-division-multiplex (TDM) signaling and supervision channel capable of handling multimode connectivity for up to 16,000 addresses. A separate channel is used because it provides net control flexibility and improved efficiency for multimedia services and permits in-process call modificaton without the need to break down established connectivities. It is conceptually compatible with the Common Channel Interoffice Signaling (CCIS) being implemented by the common carriers in accordance with CCITT signaling system No. 6 recommendations. The polled asynchronous S&S technique is being employed because it provides response to service requests in less

than one second yet minimizes the complexity and cost of each terminal interface device.

2.2.2 Digital Data Distribution Subsystem

Digital data distribution in a MIDS can be provided by a polled TDM subsystem which provides connectivity to those individual terminals which have requested digital data service by means of the common control channel. Up to 1024 data ports (i.e., terminals) can be simultaneously serviced at 600 bps with an automatically adaptive data rate in bursts up to 19.2 kbps.

The polled TDM technique is being employed for digital data distribution because it offers the capability to minimize the subscriber connect cost while providing flexibility for handling various message formats. It also permits implementation of the automatically adaptive data rate feature.

2.2.3 Video Distribution Subsystem

Video distribution in a MIDS can be accomplished in several ways. The simplest method is to establish a number of fixed channels with frequency multiplex equipment. The subscriber then selects which channel he will receive with a tuner on his terminal. This technique, which is employed in CATV systems, is satisfactory only when a limited number of video channels are required.

The multiplexing of many video channels on a single coaxial cable is being successfully accomplished daily in hundreds of CATV systems. Almost all of these systems, however, have no interactive communication capability since they lack suitable network control/signaling and supervision subsystems.

A much larger traffic handling capacity can be provided by dynamic allocaton of frequency channels only for the duration of each video transmission. Subscriber connections are established by the network control assignment of channels and digital tuning of each subscriber's remotely controlled video modem to the assigned frequency channel. The principal development required for this system is a digitally controlled broadband subscriber modem. Additional capacity increases can be obtained through use of local video framegrabbers for static video or character display images so that trunk channels can be released for reuse immediately upon transfer of each video image.

2.2.4 Voice Service Subsystem

Telephone service in a MIDS can be provided by means of either Frequency Division Multiplex (FDM) or Time Division Multiplex (TDM) techniques. The frequency multiplexing of many voice channels on a single coaxial cable has been demonstrated on a limited scale by the Collins Radio ATX-101 Decentralized Switching Telephone System.

For military applications a TDM system, however, would probably be more desirable since digitized speech signals are more amenable to the application of security techniques. A telephone subsystem for use in a MIDS could be developed using either the Bell System 64 kbps T-Carrier standards or the DoD 16/32 kbps continuous variable slope delta (CVSD) standards.

2.3 NETWORK CONFIGURATION SYSTEM DESIGN

The control and data distribution elements for a MIDS are illustrated in Figure 1. The transmission path is a wideband coaxial cable of 300 MHz bandwidth. Separate upstream and downstream cables are used to minimize mutual interference. If a single cable were used for a two-way system, carefully-engineered bi-directional amplifiers containing expensive filters to minimize amplitude and frequency distortions over long cable runs would have been required. In addition a large number of two-way interactive terminals accessing a single cable would have collectively presented a potential high source of noise to the system.

Control and data distribution signals are transmitted on separate frequency channels of the same multi-channel cable. The control channel performs the signaling and supervision function. The data distribution channel transmits messages to their proper destinations. Each Subscriber Data Buffer Unit contains a propagation-delay equalizer that is adjusted during the initial system line-up procedure. The time delay equalizers compensate for the difference in distance that exists between terminals close-in to the channel controller as compared to terminals at the far-end of the cables. The combination of the delay equalizers plus the provision of an inter-message frame gap prevents messages in one time slot from overlapping messages in adjacent time slots.

The signaling and supervision control channel terminates in a network control processor such as a PDP-11 minicomputer or equivalent. A minicomputer is required since the network is planned to eventually provide many more services than just data transmission and distribution (References 1 and 2).

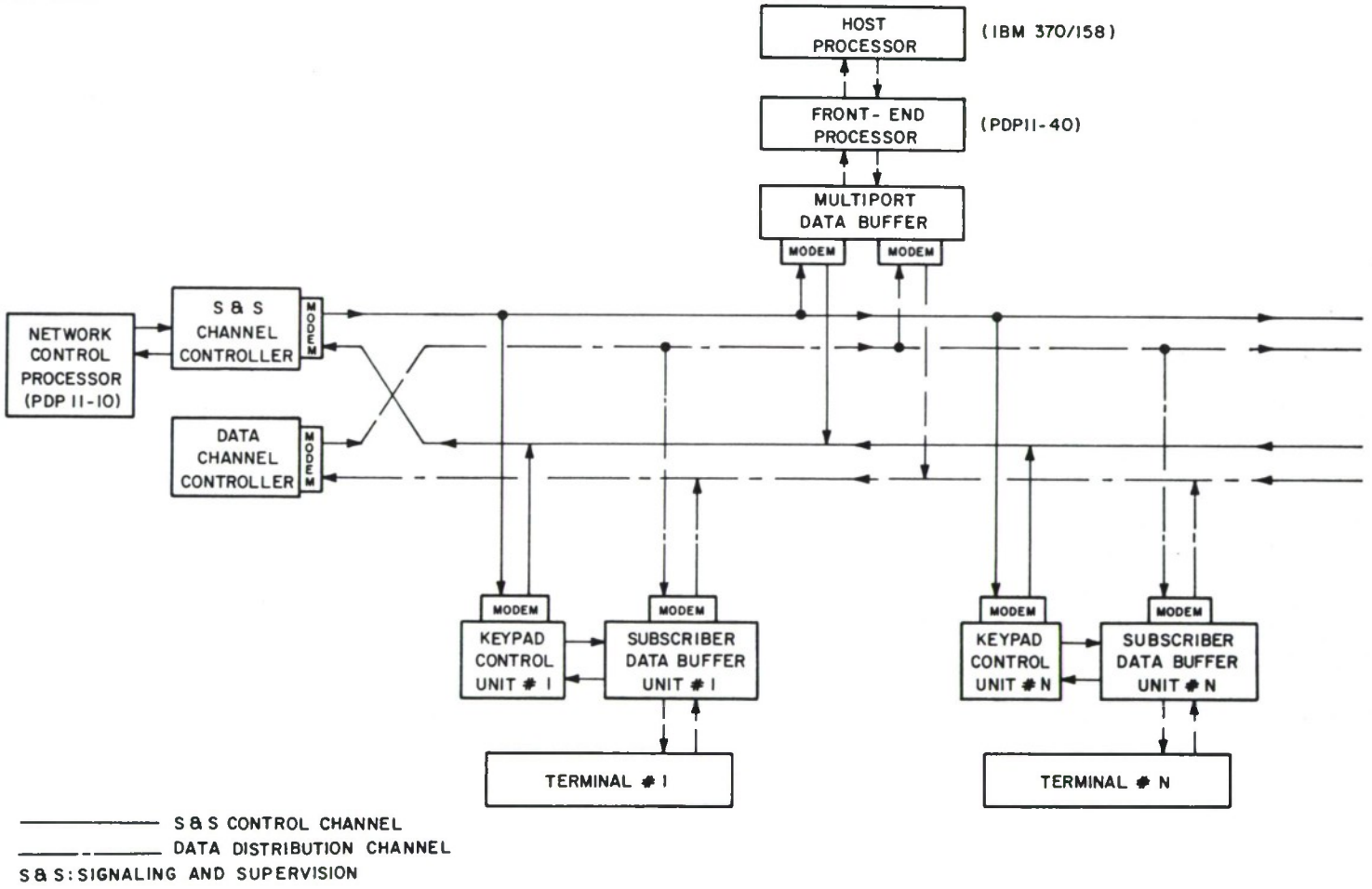

Figure 1 DATA DISTRIBUTION AND CONTROL NETWORK CONFIGURATION

2.4 SIGNALING AND SUPERVISION (S&S) CHANNEL DESIGN

The S&S control channel provides the path for accepting request-for-service signals from subscribers' terminals and for sending status and address information back to subscriber terminals. The S&S subsystem uses a form of polled, asynchronous, time-division-multiplex transmission. The polling from the S&S channel controller is initiated by a flag-for-service request from the subscriber's terminal.

The information flow over the S&S channel is illustrated in Figure 2. There are 64 signaling and supervision time groups in a time frame. The time group is divided into a flag-for-service field, a polling field and an information field. The flag-for-service field contains 256 bit times. This quantity of bit-times repeated over 64 time groups yields 16,384 bit positions. A flag-for-service technique is used to handle requests for service from any of 16,384 subscribers. Each subscriber's keypad is assigned a code (directory address) which corresponds to a unique bit position in the field of 16,384 bits in the time frame. Starting with the beginning of each time frame, the keypad logic counts each bit received on the downstream cable until its assigned bit position is reached. At this point in time, the keypad logic sends a flag-for-service pulse on the upstream cable. In the meantime the subscriber may enter his service request by depressing the appropriate keys on the keypad.

The channel controller recognizes the flag-for-service pulse because of its time position and then polls that subscriber by sending the address of his keypad in the next available polling field. When the keypad recognizes its polling address on the downstream cable, it responds by transmitting the stored keystrokes and status information on the upstream cable during the time occupied by the 48-bit information field. The channel controller accepts the keystroke/status information which conveys the subscriber's request and forwards it to the network control processor. The remaining 63 time groups in the same time frame are available for "simultaneous" servicing of other subscribers.

The network control processor then checks availability of equipment involved in the desired connection. Presuming availability,the network control processor sends the necessary indirect-address information to the keypad control unit for transfer to the Subscriber Data Buffer Unit. Data transmission between subscribers may then begin on the data distribution channel.

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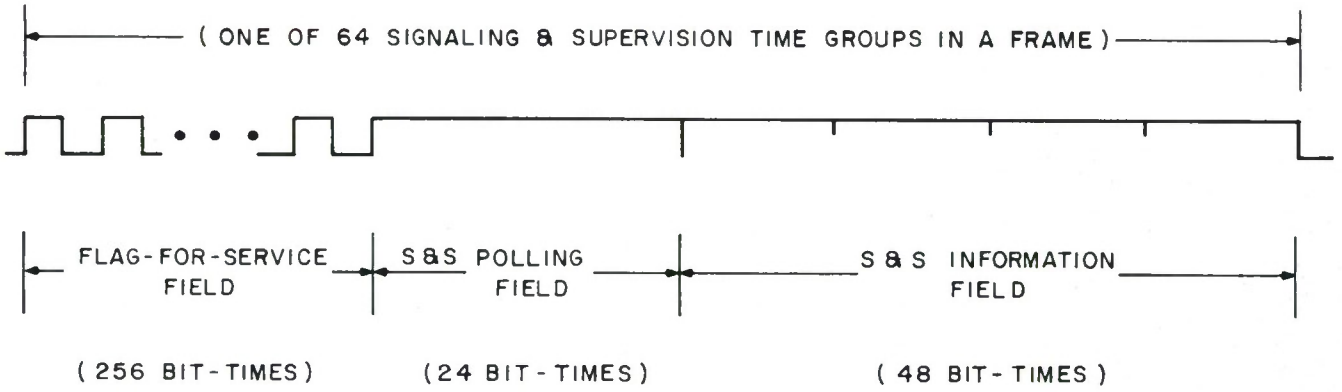

Figure 2 SIGNALING AND SUPERVISION SUBSYSTEM MESSAGE FIELDS

The message format for the S&S polling field and information field uses an 8-bit character structure. Character transmission is performed on a conventional start-stop asynchronous basis. The design of the S&S channel is described in detail in Section 3.

2.5 DATA DISTRIBUTION CHANNEL DESIGN

The digital data distribution subsystem is based on a form of polled, time-division multiplexing. This subsystem will accommodate up to 1024 simultaneous data users. The data distribution channel controller sequentially polls all 1024 addresses in its polling table. These addresses are not permanently assigned to any particular terminal and do not correspond to the fixed address of the terminal's keypad. For this reason the addresses used in the digital data distribution subsystem are called indirect addresses. The indirect addressing feature is used to allow up to 1024 terminal connections to time-share the data channel out of a population of 16,384 subscribers.

The structure of the message fields used on the data channel is illustrated in Figure 3. During the polling (transmitter) address field time the data channel controller sends on the downstream cable the address of the terminal which is expected to transmit. When the polled terminal recognizes its address, it uses the remaining 85 bit-times to send its data message on the upstream cable. The data message contains a control/receiver address field followed by an information field. The information field contains the remaining 68 bits which consist of four 16-bit words with each word followed by a single parity bit. The data channel controller passes the upstream data message to the downstream cable following the next available polling address field. During this downstream transmission the receiving terminal accepts the data messages previously inserted by the transmitting terminal. This completes a typical transmit-to-receive cycle.

In order to provide simultaneous multiple terminal access to common-user facilities such as a data processing computer, a multiport data buffer unit is being developed (see Figure 1). This multiport data buffer design is capable of providing communication between 64 terminals on the cable and a large host-processor computer. The host processor would interface to the multiport data buffer through a front-end-processor such as a PDP 11-40 minicomputer. The advantage of using the multiport data buffer unit over individual subscriber data buffer units for such access is that common circuits may be used. For example, only one set of modems is required by the multiport data buffer unit to interface the cable.

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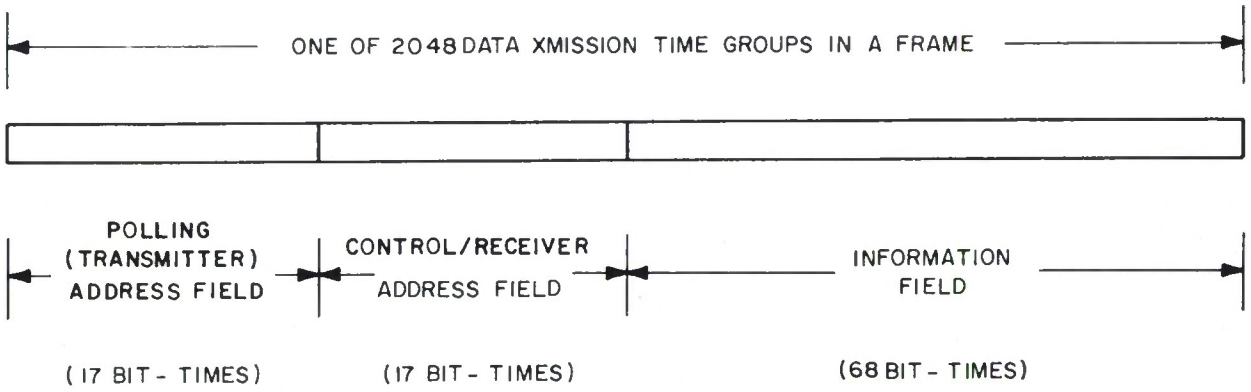

Figure 3 DATA DISTRIBUTION SUBSYSTEM MESSAGE FIELDS

Thus, the many-to-one connectivity of multiple terminals to a host computer is economically achievable.

A unique feature of the digital data distribution system is that the data rate to any particular terminal is automatically adapted to fulfill the traffic activity demands of each terminal. The adaptive data rate permits the system to automatically switch a terminal from a basic 600 bps data rate to a higher speed of 19.2 kilobits per second as demanded by terminal traffic activity. Of the 1,024 simultaneous on-line terminals any 16 pairs of terminals are permitted the higher data rate as required. The interaction of the 600 bps and 19.2 kbps data rates can be visualized as two circular polling queues shown in Figure 4. The poll address selectors within the circular queues rotate at a different speed. The 600 bps data rate terminal devices are on the low-speed selector rotating at 10.56 revolutions per second. Terminal devices requiring 19.2 kbps data rate service are temporarily assigned to the high speed selector rotating at 338 revolutions per second. Alternate interleaving of poll addresses from the two queues provides the TDM servicing of all terminals which may be active. Automatic adaptive data rate service is provided by monitoring the output buffer in each terminal interface device, thereby permitting efficient dynamic allocaton of capacity. As the output buffer fills up, the polling rate to that terminal is increased providing a high data rate transfer and a rapid screen fill time for visual display terminals. As the buffer is emptied, the polling rate decreases to a lower effective data rate. This lower data rate is sufficient to handle normal keyboard activity of 15 characters/second yet maintains terminal connectivity so that rapid data transfer can take place without need for reestablishing a connection for each transmission. The design of the data distribution channel is described in detail in Section 4 and the traffic-handling capacity is analyzed in Appendix A.

2.6 DESIGNING WITH MICROPROCESSORS

2.6.1 Logic Design Considerations

From the preceding system description and the diagram in Figure 1 it is evident that both the signaling and supervision control channel and the data distribution channel will involve a large number of logic functions. The traditional design approach used to implement these functions would be either with hard-wired logic, a minicomputer, or a combination of both to perform the various system element functions. The minicomputer approach would be used when there was sufficient arithmetic computation and storage required. The hard-wired logic approach provides an intrinsically faster logic

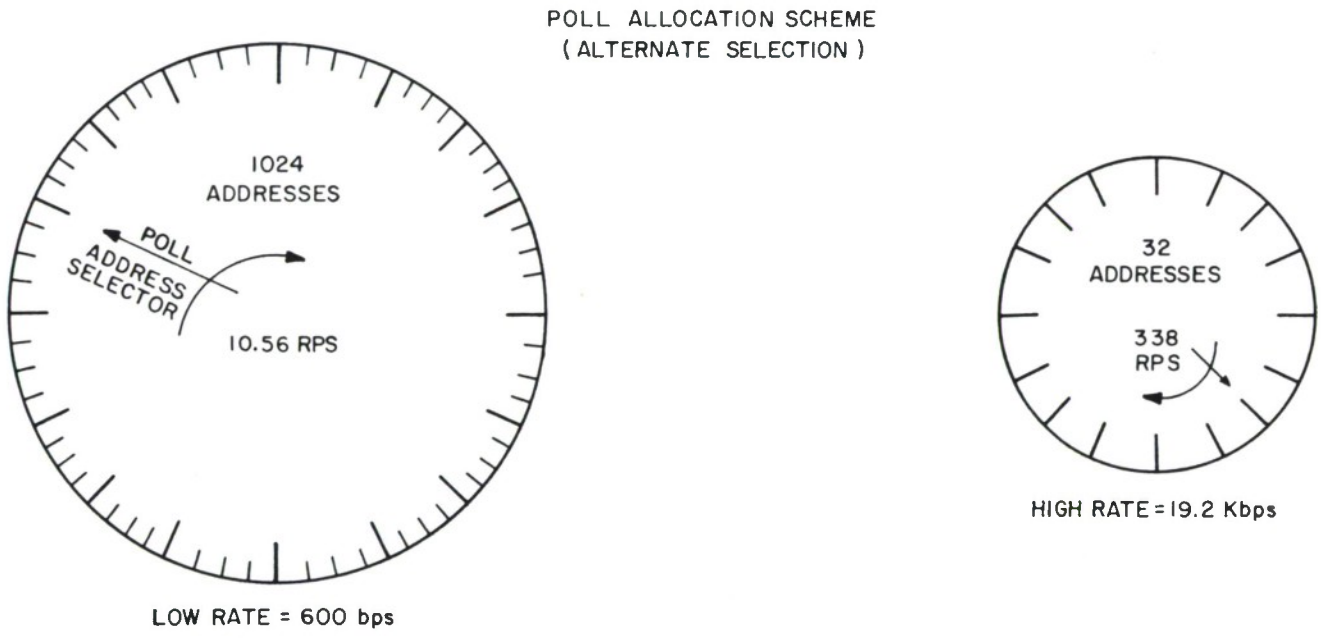

Figure 4 SELF-ADAPTIVE DATA RATE POLLING ANALOG

system. This is based on the fact that hard-wired logic is not limited to serial implementation of logic as in stored-program computers. Thus, there can be many parallel processes being performed simultaneously with hard-wired logic. The disadvantage of hard-wired logic is the duration and cost of the design, procurement, fabrication, and test cycles. If the unit is to be used in very high volume production, then custom large scale integrated (LSI) circuits may be used to overcome some of the costliness of the hard-wired logic approach. However, if day-to-day operation in the "field" later produces a requirement to change the logic, the expense of the manufacturing modification to the LSI chip may easily offset the initial gain. Changes in etched-foil circuit cards are likewise difficult and expensive.

An attractive economical alternative to the hard-wired logic approach or the minicomputer approach has recently become available with the introduction of microprocessors. Although microprocessors are implemented with serial logic as in any computer, their very small size and low cost make them a first choice consideration as a desirable system design element. Where speed of processing is critical, a few conventional integrated-circuit logic elements may be interfaced with the microprocessor to handle the high speed functions or alternatively, two or more microprocessors may be used. The low cost of the microprocessors makes this practical. Even if the hardware cost of the multiple microprocessors came up to the level of the hard-wired logic assemblage, the overall implementation cycle from design to test is, in general, much shorter using the microprocessor approach. Additionally, the microprocessor approach offers ease of system modification. The judicious use of microprocessor elements therefore offers the distinct possibility of improved designs with lower overall costs and smaller package size.

2.6.2 Digital System Functional Blocks

Digital microprocessor systems are characterized by five basic functional building blocks. As illustrated in Figure 5 these blocks include the following functions: Memory, Arithmetic Logic Unit, Input, Output, and Control and Timing. Memory is used to store both data files and program sequences. The Arithmetic Logic unit performs the arithmetic and the Boolean logic functions required by the system application. The input functional block is used to interface such input devices as keyboards, data demodulators, transmission line receivers, etc. The output functional block interfaces such output devices as printers, indicators, data modulators, transmission line drivers, etc. The control and timing block operates the steering circuits that interconnect the other system elements. The control sequence causes the actual digital

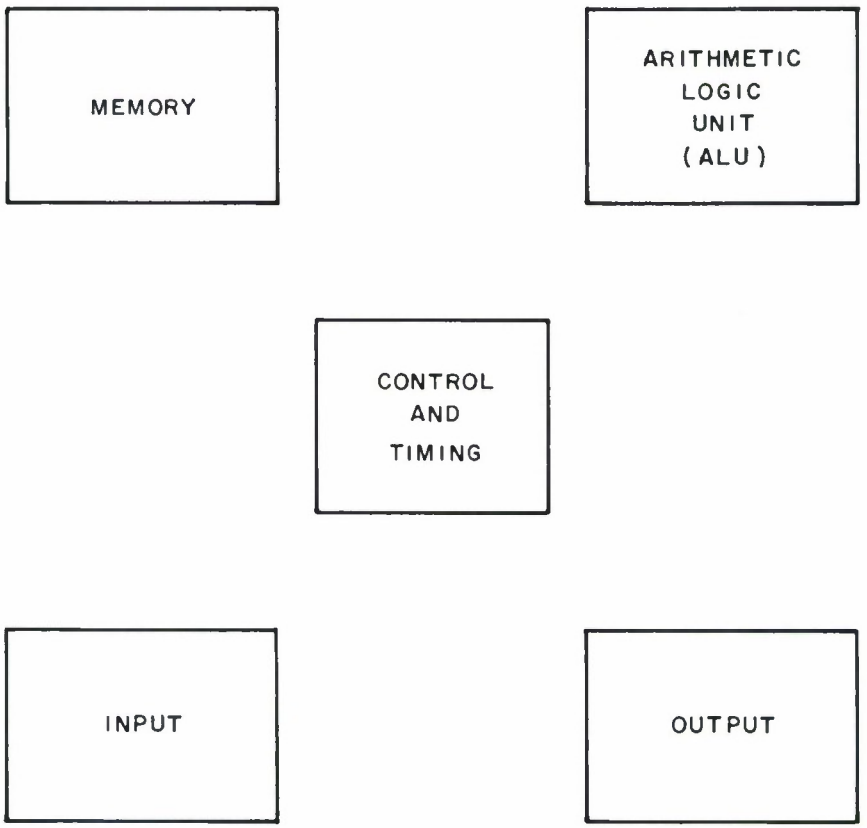

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Figure 5 DIGITAL SYSTEM FUNCTIONAL BLOCKS

control algorithm for the particular system application to be executed. The timing circuits assure that the information will be gated between the various system elements in a non-hazardous fashion, e.g., so that flip-flops will only change state at the time of a clock pulse. As the program memory contains the complete instruction sequence, the digital system is said to be a stored-program machine and the operations can be readily modified by changing the contents of memory.

2.6.3 Microcomputer Chip Set

In digital computers the arithmetic logic unit and the control and timing circuits are generally grouped together in the same hardware area. This grouping is called the central processing unit (CPU) of the computer.

The term microprocessor has both a narrow and a broad connotation. In its narrow connotation it means central processing unit. In its broad connotation it means the entire microcomputer set. Most microprocessor manufacturers offer a family of integrated circuits to perform the entire digital system function. Since the integrated circuit is formed from a silicon chip, the circuits are often called "chips". The grouping of the digital system functions into a typical microcomputer chip set is illustrated in Figure 6. One of the chips is the CPU chip. This chip is often referred to as the microprocessor chip. Another chip is the memory chip. Depending on memory storage requirements several memory chips may be needed to satisfy a system application. A third chip is the input/output chip. Depending upon the number of peripherals to be interfaced, this could be one or more chips.

It is interesting to note that the memory chip provided the impetus for the entire microprocessor development. The chip manufacturers achieved a very large reduction in size for the memory circuits. In order to promote the use of these memory circuits, their development effort was turned to the task of producing a central processing unit on a chip which employed the same technologies and production facilities. This development started with a four-bit central processing unit for hand-held calculators, then advanced to an 8-bit CPU unit; even 16-bit CPU units are available today.

2.6.4 Microcomputer Architecture

The microprocessor architecture has followed the trend established by modern minicomputers. It uses a bus structure to interconnect the various digital system functional elements as

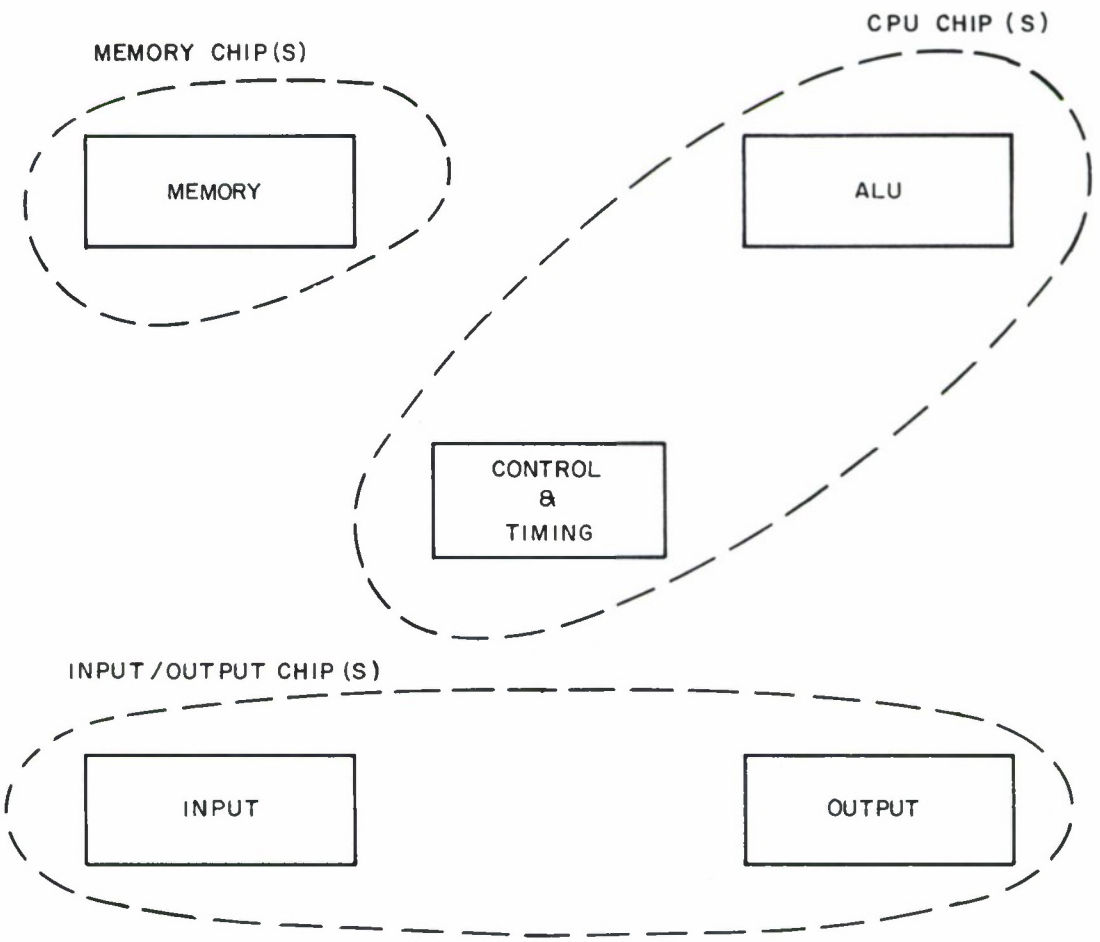

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Figure 6 MICROCOMPUTER CHIP SET

illustrated in Figure 7. The microprocessor bus, itself, is merely a set of parallel lines used to transfer the data and control signals. For example, in a 4-bit microprocessor configuration, four lines are utilized on a time-sharing basis to distribute memory address, instructions, and data in 4-bit groups, each in its own sub-cycle of time.

In most microprocessors the input/output units have an interrupt capability that permits the CPU to perform logic and arithmetic operations without checking the state of the peripherals. When a peripheral device requires service, the input/output unit signals the central processing unit via an Interrupt line. The CPU then suspends its normal operation and services the peripheral unit.

A separate clock-circuit chip is often used as the source of accurate timing for the CPU which in turn maintains the synchronism for the entire set of microcomputer elements.

In the memory area the microprocessor architecture usually distinguishes between Random Access Memory (RAM) requirements and Read Only Memory (ROM) requirements. The random access memory chip contains volatile data that will be entered into memory at the start or during execution of the program. Most of this data is of a variable nature that will be changed during the processing of the various transactions. Microprocessors, in replacing hardwired logic systems, require not only an immediate start up with application of power, but also require a permanent program memory which will not change unintentionally with the passage of time. Hence, the need for Read Only Memory (ROM) elements is dictated for program storage.

The integrated circuit devices use a metal oxide silicon (MOS) fabrication technique. MOS is a technique that consumes minimum power thus providing the ability to put up to 2,000 logic gates on a chip. The older and more conventional TTL logic, although faster, uses more power because it has resistive components in the chip. Some vendors are offering TTL CPU chips in four-bit slices. The slices can be assembled into 8-bit or 16-bit central processing units. Since each slice is an individual chip, the heat dissipated in a 16-bit CPU is distributed among 4 chips. The choice of using a MOS CPU chip or a set of TTL bit-slice chips is a design trade-off between speed and quantity of chips. Recently a new technology called integrated injection logic (IIL) has been developed (Reference 3). This technology combines the low power dissipation of MOS with the high speed performance of TTL and promises to permit even more applications for microprocessors in the future.

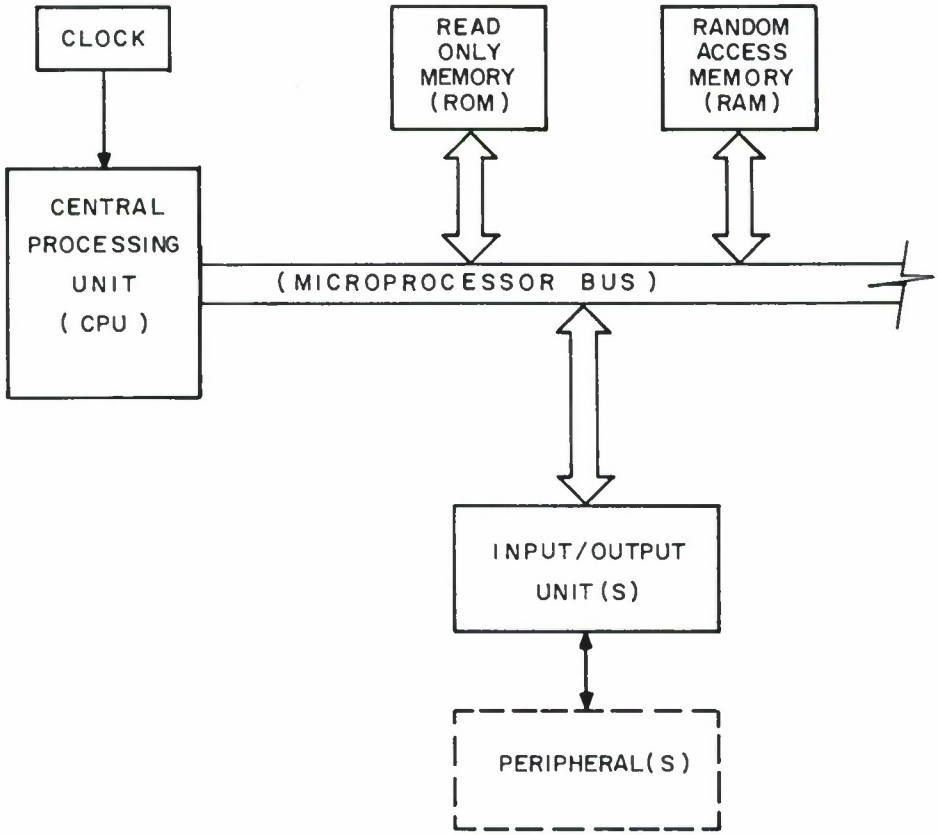

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Figure 7 SIMPLIFIED MICROCOMPUTER ARCHITECTURE

2.6.5 Microprocessor Application to MIDS

In the MIDS network configuration of Figure 1, there are system logic elements that process 4 bits, 8 bits, or 16 bits with various speed or throughput requirements. A range of microprocessors is now available to meet these applications. For example the keypad control unit transmits 15 different keystrokes. Since up to 16 keystrokes can be encoded by 4 bits, this is an obvious application for a 4-bit microprocessor. Furthermore, and perhaps most importantly, a 4-bit microprocessor has sufficient speed characteristics to process the major control activities associated with the keypad unit. The MIDS laboratory development system is using the Intel 4040 four-bit MOS microprocessor system for the Keypad S&S subsystem (Reference 4).

At the headend of the cable, a PDP-11 minicomputer provides the signaling and supervision control for up to 16,000 subscribers. In earlier designs the hardware interface between the cable and the minicomputer was performed by a hard-wired logic controller. In the MIDS laboratory development system a 16-bit microprocessor is being used to interface with the 16-bit PDP-11 minicomputer. A National Semiconductor Corporation 16 bit MOS microprocessor called the Processing And Control Element (PACE) is being used for this application (Reference 5).

The MIDS system connects a terminal to the cable through a Subscriber Data Buffer Unit. Since data transmission is character oriented, an 8-bit microprocessor could be used. In a large-scale commercial network an 8-bit microprocessor would probably be chosen for this application. However, for the MIDS laboratory development effort the same 16-bit microprocessor used for the channel controller is being used for the data buffer unit in order to compress the system development cycle. The use of the 4-bit and the 16-bit microprocessor is sufficiently versatile to provide the technical information necessary to establish meaningful system specifications and to illustrate the application of microprocessors as system design elements.

SECTION III

SIGNALING AND SUPERVISION SUBSYSTEM

3.1 GENERAL

The Signaling and Supervision Subsystem provides the control for the MIDS network. The following basic control functions are performed:

- o Handle requests for connectivity
- o Authenticate request and requestor
- o Ascertain availability of equipments
- o Establish connectivity
- o Monitor connectivity
- o Report status

The Signaling and Supervision subsystem operates over a channel of the cable that is separate from the channels providing the subscribers information distribution services. This feature is equivalent to out-of-band, common-channel signaling in the commercial telephone network. The S&S channel permits the MIDS subscriber to modify connections without disturbing any information distribution transaction already in progress. Similarly changes in equipment status are monitored and reported automatically over the S&S channel regardless of the state of the subscriber's connections.

The S&S subsystem contains several major functional elements including the Network Control Processor (NCP) and its operational software, the Channel Controller, and Keypad Control Units that provide the interface to the subscribers' terminal equipments. The Channel Controller is collocated with the Network Control Processor at the "headend" of the cable. Communication between the Channel Controller and the Keypad Control Units is based on a form of polled, asynchronous time-division-multiplex transmission.

Several improvements have been made in the details of the S&S subsystem design as described in Reference 1. The User/System Control Information Flow description has been expanded to include the addition of two new status lamps, i.e., the Dial lamp and the Call Active lamp. The S&S Channel Timing description has been revised due to the addition of a flag-for-service field in the S&S

message structure. The use of the flag-for-service technique reduces the bandwidth required for the S&S channel. The Network Control Processor description contains two minor changes to the software. The original timing and sizing analyses included in Reference 1 have not been affected. The S&S Channel Controller is being redesigned around a 16-bit microprocessor. Only a summary description is provided since the design is still in progress. The S&S Keypad Control Unit also is being redesigned to employ a 4-bit microprocessor and this is essentially complete; a detailed description is presented. The Keypad Control Unit Modem is also briefly described.

This section describes the following aspects of the MIDS network control subsystem:

- o User/System Control Information Flow
- o Signaling and Supervision Channel Timing
- o Network Control Processor
- o S&S Channel Controller
- o S&S Keypad Control Unit
- o Keypad Control Unit Modem

3.2 USER/SYSTEM CONTROL INFORMATION FLOW

The keypad with its associated status lamps is the primary interface between the user and the signaling and supervision subsystem. The layout and markings of the keypad are illustrated in Figure 8. A conventional 10-button keypad with six additional function keys is utilized. The six status lamps indicate the progress of the dialing sequence. The lamps are color coded for ease of reference by the user. In addition to the ten numeric keys the following function keys are provided:

S: Service Package
C: Clear Keystrokes
D: Disconnect
R: Redial Call
M: Modify Call

The sixth function key is unassigned and is available for future use.

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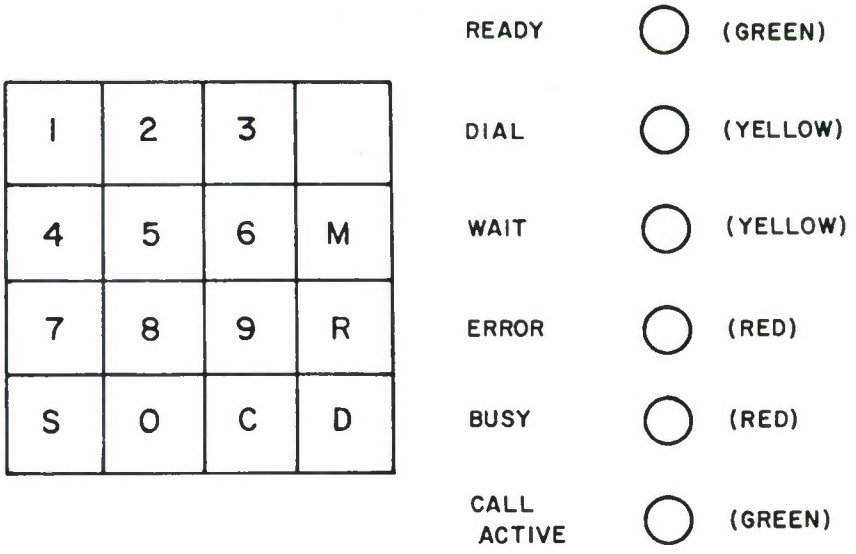


LEGEND

S : SERVICE PACKAGE
C : CLEAR KEYSTROKES
M : MODIFY CALL
R : REDIAL
D : DISCONNECT

Figure 8 KEYPAD & INDICATOR LAYOUT

Six indicators are used to present status and guide user response. Four are similar to the existing system, that is, READY, WAIT, ERROR, and BUSY. Two new indicators for Dial and Call Active have been added. The use of the indicators is summarized as follows:

READY: S&S system ready for user input.

DIAL: User to continue to dial.

WAIT: Call being processed.

ERROR: Dialing error.

BUSY: Called party busy.

CALL ACTIVE: Data connection complete and acknowledged.

The sequence of actions between the user and the keypad is illustrated in Figure 9. When the S&S subsystem is initialized by the Network Control Processor, the READY lamps at all of the keypads are turned on. When a user depresses a key, the resulting keystroke is collected by the S&S subsystem poll. The Keypad Control Unit may store many keystrokes in its own buffer before transmitting to the Network Control Processor, hence, the designation keystrokes in the flow diagram. The S&S subsystem checks first to see if the user has dialed either a CLEAR, a DISCONNECT, or a REDIAL. If a user has dialed a CLEAR, the S&S subsystem clears all prior keystrokes from memory and turns the READY lamp on. If a subscriber presses DISCONNECT, the S&S subsystem disconnects all prior connections and lights the READY lamp. When a subscriber presses REDIAL, the S&S subsystem will attempt to make the connection previously requested by the user. As each keystroke is received the S&S subsystem checks to see if it is the last keystroke of a legitimate dialing sequence. When the last keystroke is so received, the S&S subsystem lights the WAIT lamp which is an indication to the user that he is working into an active system. It does not necessarily mean that the subscriber has to wait to do anything else. The S&S Network Control Processor then processes the call request. If a user has made an invalid request or a detectable error in dialing, the ERROR lamp is lit. The ERROR lamp however is timed out by the system so that the READY lamp will illuminate after a predetermined time. If the called party is busy or out of service, the S&S subsystem will light the BUSY lamp on the calling party's keypad. It will then proceed to time out this busy lamp, and after a predetermined time, it will again light the READY lamp. If, however, the necessary equipments are available the S&S subsystem will complete the connection at both

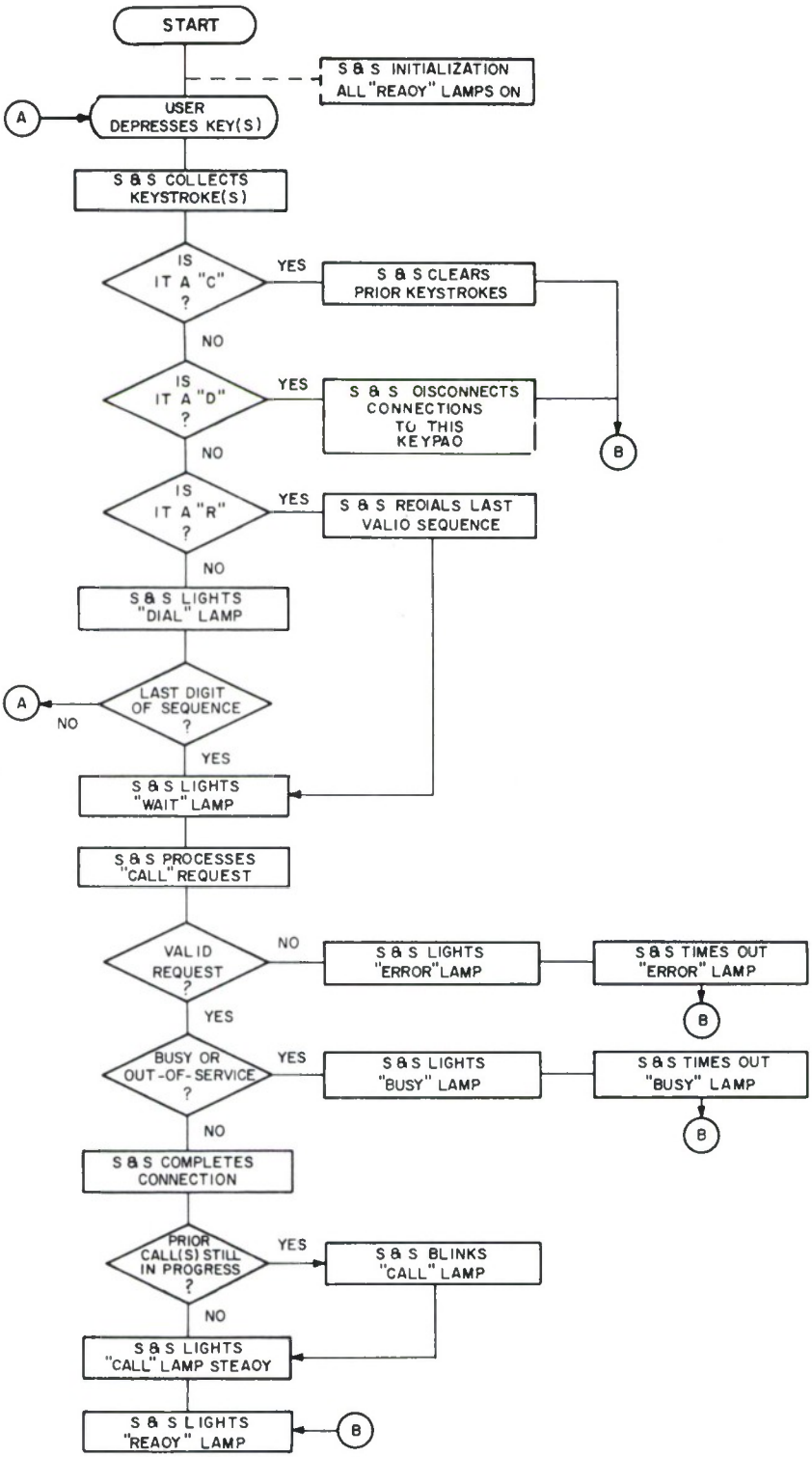


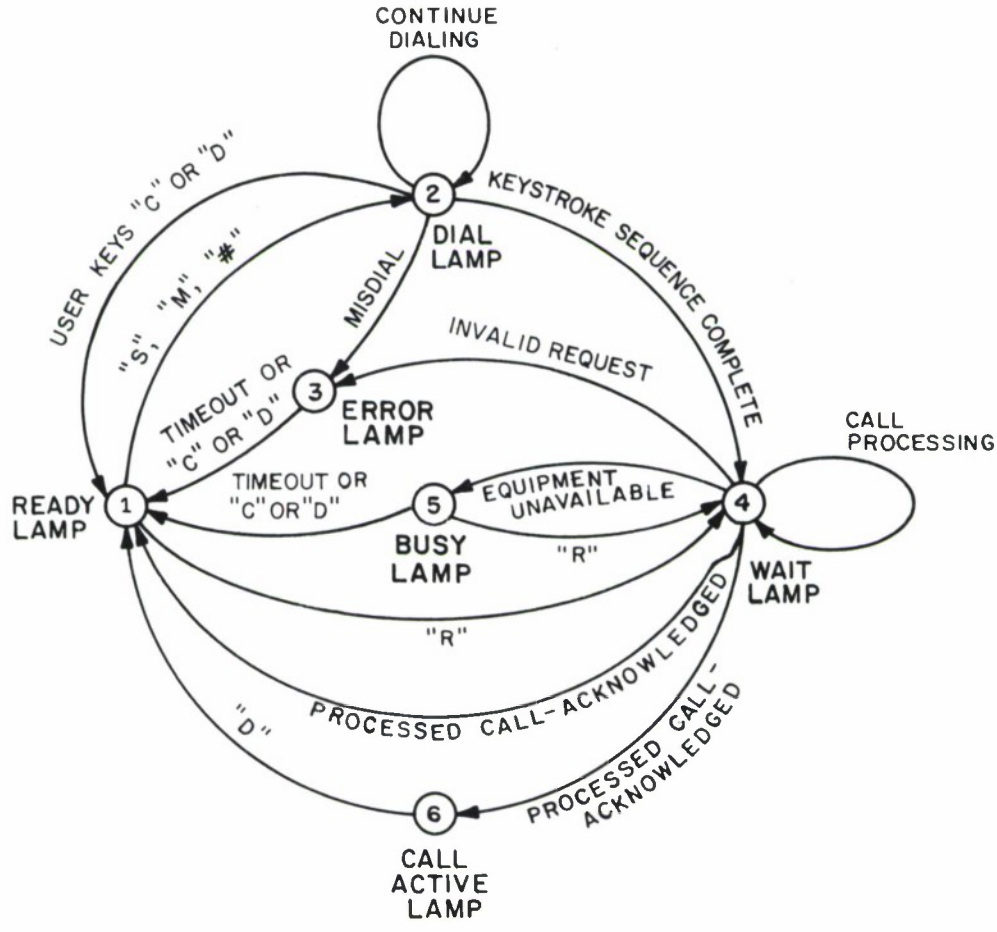
Figure 9 DIALING SEQUENCE

the calling and called party's keypads. If this connection is the initial call from this keypad, the CALL ACTIVE lamp would be lit by the S&S subsystem. Before lighting the CALL ACTIVE lamp however the S&S subsystem checks to see whether a previous call from this Keypad is still in progress. If a previous connection has already been established for a different service package, then the CALL lamp would already be lit. If so, the S&S subsystem will cause the CALL lamp to blink before returning it to a steady state. The S&S subsystem also lights the READY lamp to indicate to the user that it is ready for another dialing sequence.

Another diagram for describing states and transitions is the state diagram. The state diagram for the six indicator lamps associated with the keypad is illustrated in Figure 10. Starting with the READY lamp illuminated (1), the user may depress a digit key, service package key "S", or the call modification key "M". This action will cause the DIAL lamp to illuminate (2). It will stay on during the dialing sequence unless the CLEAR or DISCONNECT button is depressed which returns the keypad unit to the READY state. When the keystroke sequence is complete, the WAIT lamp comes on (4). However, during the dialing sequence, if an invalid character is dialed or if the inter-digit arrival time is determined by the processor to be too long, the user is timed out and an ERROR lamp comes on (3). After a short interval the ERROR lamp is turned off and the READY lamp is turned on by the Network Control Processor. Assuming the dialing sequence has advanced to the WAIT lamp being illuminated, the call is processed and if it cannot be completed due to called party or common equipment in a busy condition or out of service, the BUSY lamp comes on (5). The BUSY lamp is eventually timed out and the READY lamp illuminates (1). The user may redial the previous sequence by pressing the REDIAL Key ("R") while the BUSY lamp is still on or even after it goes off. The keypad unit will return to the WAIT state and the processor will automatically attempt to complete the connection again. Assuming the processor has completed the call, then the CALL ACTIVE lamp illuminates (6). For simplicity in the state diagram the blinking of the CALL ACTIVE lamp for additional dial sequences is not indicated since it has already been described in the flow chart sequence. The CALL ACTIVE state is terminated when the user depresses the DISCONNECT button. The S&S system then extinguishes the CALL ACTIVE lamp and turns on the READY lamp if it is not already on.

3.3 SIGNALING AND CHANNEL TIMING.

As described in Section 2.2, the Signaling and Supervision subsystem uses message time frames for transmitting information on



LEGEND

C: CLEAR KEYSTROKES
D: DISCONNECT
S: SERVICE PACKAGE
M: MODIFY CALL
#: DIGITS Ø THROUGH 9
R: REDIAL

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Figure 10 KEYPAD LAMP INDICATOR STATE DIAGRAM

the downstream cable and receiving information on the upstream cable. The details of this message structure are illustrated by the telescoping levels in Figure 11. The top level of the diagram shows three message time frames interposed by two frame gaps. Each time frame is 0.839680 seconds in duration and contains 64 time groups. The intermessage frame gap is 960 microseconds. The transmission rate is 25 kbps.

The middle level of tne diagram shows a single time group subdivided into its three constituent fields. The first field is designated the "flag-for-service" field and contains 256 symmetrical square-wave pulses. The second field is the polling field containing 16 bit positions. The first two bits of this field are control bits while the last fourteen bits are the address bits for the keypad being polled. The control bits are decoded as follows:

00 - Interrogation Poll: Send your keystroke/status information.

01 - Command Poll: Set receiver and transmitter address.

10 - Command Poll: Set status lights.

11 - Unassigned: (Available for future use.)

The third field is the S&S information field which contains 48 bit times consisting of 32 information bits , 4 parity bits, 4 start bits and 8 stop bits.

The bottom level of the diagram shows one of the two 16-bit words in the S&S information field received by the S&S Channel Controller from the PDP-11 Network Control Processor. The actual transmission of the S&S information field, however, is organized on a character basis. Each character contains eight information bits of 40 microseconds duration which corresponds to one byte of a two-byte minicomputer word. Character transmission is performed on a conventional start/stop asynchronous basis. Each character also contains a parity bit for error checking purposes. The information field contains such items as the data buffer receiver and transmitter addresses or status light controls, depending on which command poll was used. In the case of an interrogation poll the information field is essentially void on the downstream cable; however, it does contain the keystroke and station status (in or out of service, etc.) on the upstream cable.

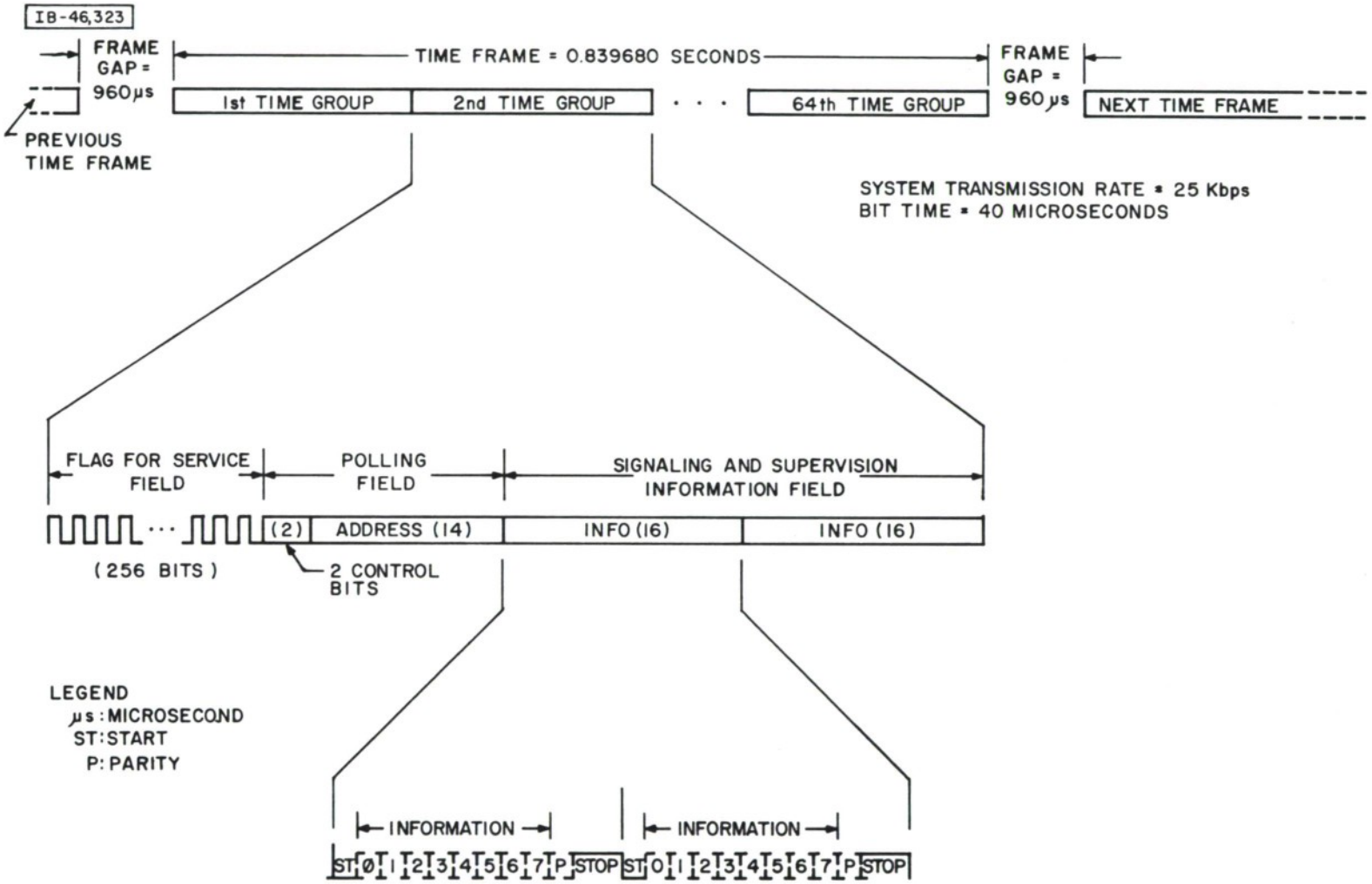

Figure 11 SIGNALING AND SUPERVISION SUBSYSTEM MESSAGE TIME FRAME

The sequence of operations between the S&S Channel Controller and a keypad control unit is illustrated in Figure 12. The diagram is divided into three subsequences to emphasize that the flag-for-service field and the polling address fields are not part of the same time group. These illustrations visualize the waveforms as they would appear to move past an observer at a specific keypad. In addition the diagram shows what information is sent on the upstream cable by the keypad control unit in response to signal information received on the downstream cable.

During the flag-for-service subsequence all keypad control units receive the 256 square wave pulses as indicated in Figure 12a. If Keypad Number 27 is requesting service, the flag-for-service logic counts up to pulse number 27 and causes a flag pulse to be sent on the upstream cable, completing the flag-for-service subsequence.

When the S&S Channel Controller detects the flag-for-service pulse from Keypad #27, it initiates an interrogation poll subsequence (Figure 12b) by inserting the polling address of keypad number 27 in the next available time group. It also sets the two control bits in the polling field to "00". The tail-end of a flag-for-service field is shown in the diagram followed by the two control bits and polling address number 27. The data receiver circuitry in the Keypad Control Unit receives the address and control bits and interrupts the microprocessor to process the information. The address recognition function is performed in the microprocessor software. To permit time for executing this compare function, transmission on the upstream cable is delayed until detection of the subsequent polling field. The keystroke and/or status information is sent via the upstream cable to the S&S Channel Controller which transfers this information to the Network Control Processor, that is, the PDP-11/10 minicomputer.

After the PDP-11/10 processes the information, it sends a command-poll message to the Keypad Control Unit. The command poll subsequence is illustrated in Figure 12c. When the Keypad Control Unit sees the tail end of the flag-for-service pulse stream it decodes the polling field and recognizes its polling address, Number 27. The control bits "01" are decoded as a command poll containing information for its own status indicators, such as turning on the "dialing-in-progress" light or the WAIT light.

Once all the keystrokes have been collected and assuming that data service was requested, the Network Control Processor will then send a command poll to the Keypad Control Unit similar in format to that indicated in Figure 12c. However the code will be "10" and the information portion of the message will contain the transmit and

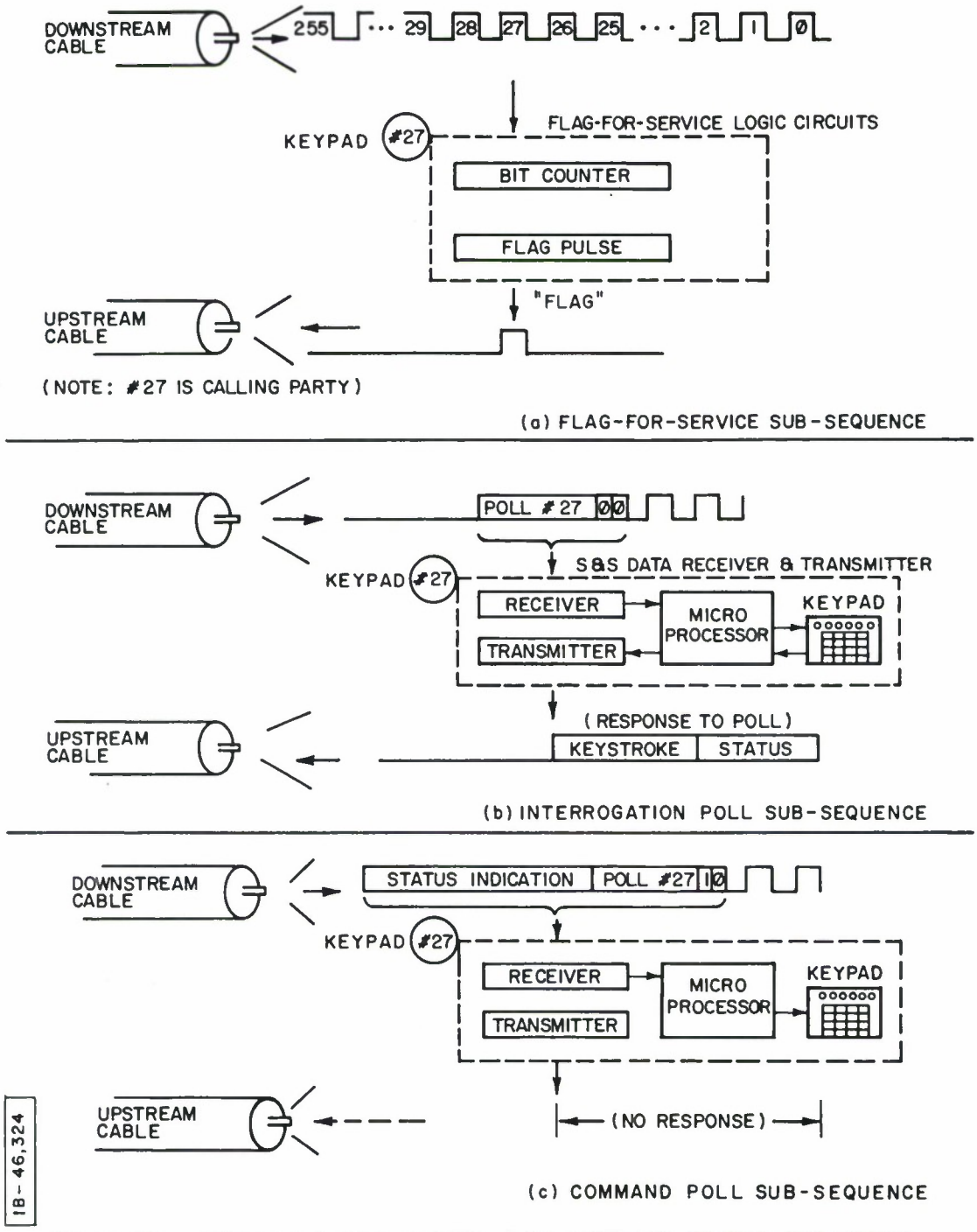

Figure 12 SIGNALING AND SUPERVISION MESSAGE TIMING SEQUENCE

receive indirect addresses for use by the MIDS data distribution subsystem.

3.4 NETWORK CONTROL PROCESSOR (NCP)

The network control processor function is performed by a PDP-11/10 minicomputer. The equipment configuration and software programs used by the PDP-11/10 for the network control function are based on a modification of the Network Control Program (NETCOP) extensively described in Reference 1. Since only minor modifications have been made to NETCOP, a complete description is not reprinted in this document.

The software modifications are as follows: The first change is implementation of the terminal equipment status reporting feature. The original NETCOP had provision for storing the status of each terminal; however, the program code to perform the status monitoring was not developed. Specifically, as each keypad is interrogated as part of the system initialization procedure the status of each terminal is stored in the existing User Data Table. In addition when a terminal goes off line, runs out-of-paper, etc., the terminal's keypad control unit sends the change-of-status information to the Network Control Processor for updating the User Data Table. Another change is required by the introduction of indirect addressing in the data distribution subsystem design. Since the S&S subsystem must store 512 indirect addresses, a 512 word table is required. The 512 indirect addresses in the table actually represent 1024 terminals. Only 512 words need be stored because connections are made on a duplex basis and the addresses of the duplex pair are always separated by the numeric 16. The addition of the DIAL and CALL ACTIVE lamps at the keypads also require minor changes in the network control program. Similarly the S&S input program, SASI, also requires minor revisions to handle an input message with up to three keystrokes instead of just one as in the previous system. The addition of status reporting plus other system features were anticipated in the original NETCOP design. As a result ample storage was allocated to these features in the original sizing and timing analysis. Hence the changes described above do not affect the sizing and timing analysis described in Reference 1.

3.5 SIGNALING AND SUPERVISION CHANNEL CONTROLLER

The Signaling and Supervision Channel Controller provides the interface between the Network Control Processor (PDP-11) and the upstream and downstream coaxial cables as shown in Figure 1. The S&S Channel Controller shown in Figure 13 is structured around a 16-

bit microprocessor which was chosen for ease of interfacing with the 16-bit PDP-11 minicomputer. The Channel Controller provides the following functions:

- o Performs the flag-for-service sequence
- o Performs the initial interrogation poll sequence
- o Manages the data transfer between the network control processor and the digital data channel for all subsequent polling sequences

The flag-for-service subsequence is controlled by the Flag-For-Service Timing/Counter block as indicated in Figure 13. The Flag-For-Service Timing/Counter circuit sends a pulse train of 256 pulses (flag counts) via the OR gate and Modulator to the downstream coaxial cable. The Flag-For-Service Detector monitors the upstream cable to detect "flag" pulses sent by Keypad Control Units. The pulse arrival times are matched against a counter to determine which Keypad Control Unit generated the upstream "flag" pulse. The pulse count is then converted to a keypad address and transferred to the microprocessor via the microprocessor bus. The microprocessor then initiates polling of that specific keypad by sending the address downstream in the next available time group. This is accomplished by transferring the address in bit-parallel form to the asynchronous data transmitter. With each 14-bit address, two control bits are also sent. For the initial polling sequence the control bits are both zeros as described in Section 3.2. The asynchronous data transmitter accepts the 16-bits in parallel from the microprocessor bus and for convenience in transmission divides the 16-bits into two 8-bit information characters and transmits the characters, bit-serial, in the start-stop asynchronous mode. Up to this point the operation of the Channel Controller is independent of the Network Control Processor, thus permitting the Network Control Processor to execute its own internal programs without excessive interrupts.

Upon receipt of the initial addressed poll the Keypad Control Unit sends back keystroke or status information to the S&S Channel Controller. The information is detected by the S&S Data Detector and transferred to the Asynchronous Data Receiver. The Asynchronous Data Receiver then interrupts the microprocessor and transfers the information to the microprocessor which in turn interrupts the Network Control Processor (PDP-11) to transfer the keystroke information or status information. Subsequent keystroke or status information is accepted by the Channel Controller and continues to be passed to the Network Control Processor PDP-11 until enough information has been received to act on a subscriber's request. At that point the PDP-11 processes the request and sends the

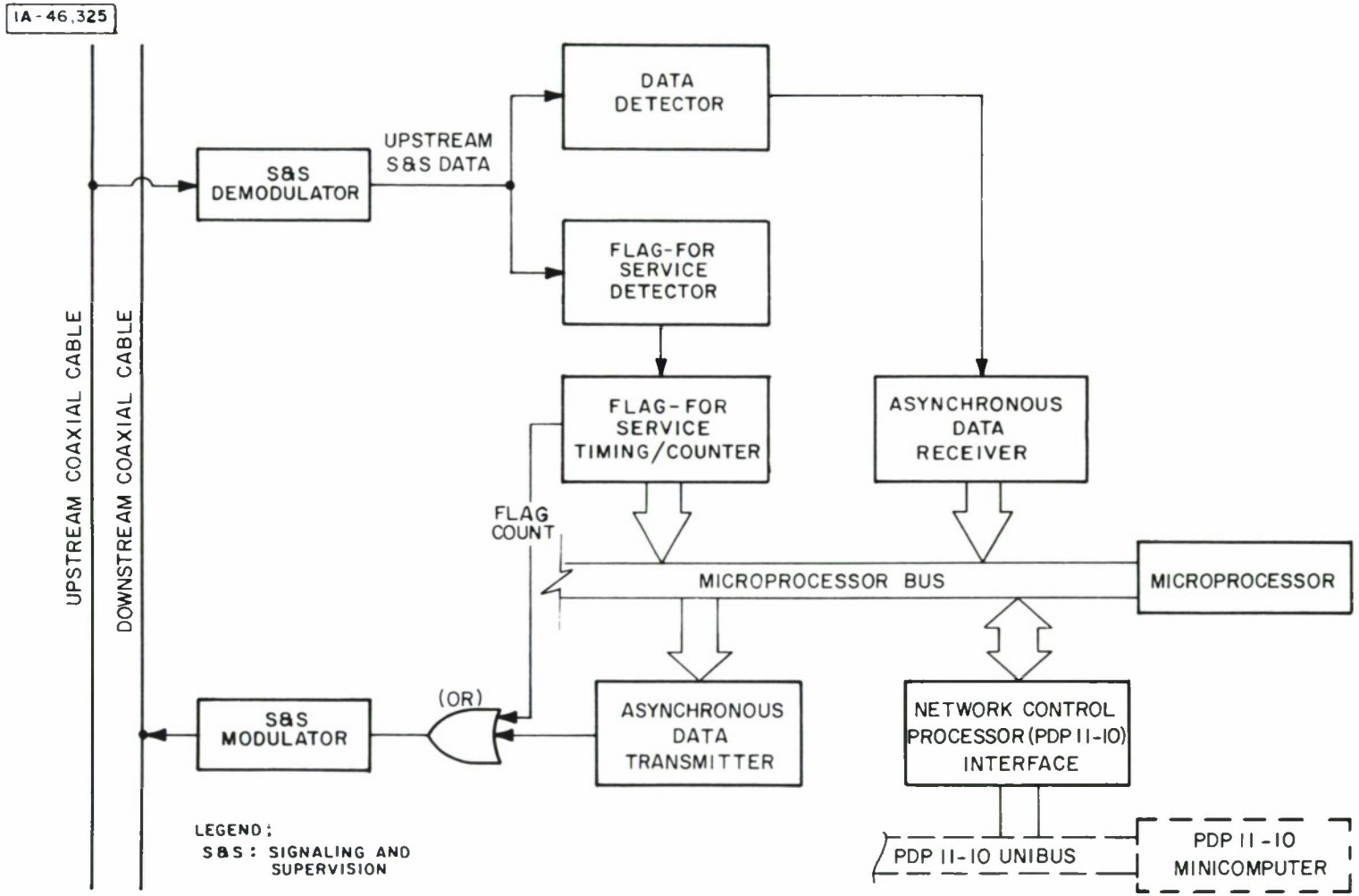

Figure 13 SIGNALING & SUPERVISION SUBSYSTEM CHANNEL CONTROLLER

appropriate control and status information downstream via the S&S Channel Controller.

3.6 SIGNALING AND SUPERVISION KEYPAD CONTROL UNIT

The Keypad Control Unit provides the man/machine interface with the signaling and supervision subsystem via the keypad and its associated status lamps. The Keypad Control Unit consists of logic circuitry and a cable modem for interfacing the keypad and indicator circuits to the coaxial cable. It also contains the interface between the S&S subsystem and the Subscriber Data Buffer Unit (Section 4.3)

The Keypad Control Unit is subdivided into the six functional blocks shown in Figure 14.

- o Flag-for-Service Logic
- o S&S Data Transmitter and Receiver
- o Operator Interface
- o S&S Microprocessor
- o Data Buffer interface
- o Cable Modem

The serial bit stream from the downstream cable is converted from RF to DC voltage levels by the demodulator portion of the cable modem. The DC-level bit stream is supplied to the Flag-For-Service logic and the S&S Data Transmitter and Receiver logic. The Directory Address Comparator counts the pulses in the flag-for-service field in the downstream message until it reaches a count comparable to the address number of its own keypad control unit. At this time it changes the input level to the AND gate shown in the flag-for-service logic block. If there is also keystroke/status information residing in the keypad unit, the AND gate is enabled which originates a flag-for-service. The flag-for-service pulse is thus applied to the OR gate shown in the S&S Data Transmitter and Receiver block. This pulse passes through the OR gate to the modulator which converts it to RF for transmission on the upstream cable. It is received by the S&S Channel Controller which completes the flag-for-service subsequence.

When the flag-for-service field of the downstream S&S message has reached its terminal count of 255, the Keypad Control Unit disables the Flag-For-Service logic and enables the S&S Data Transmitter and Receiver. The Asynchronous Data Receiver (ADR) then accepts the next six 8-bit characters. After the receipt of the first character, the ADR sends an interrupt signal to the microprocessor. The eight bits are transferred in two successive

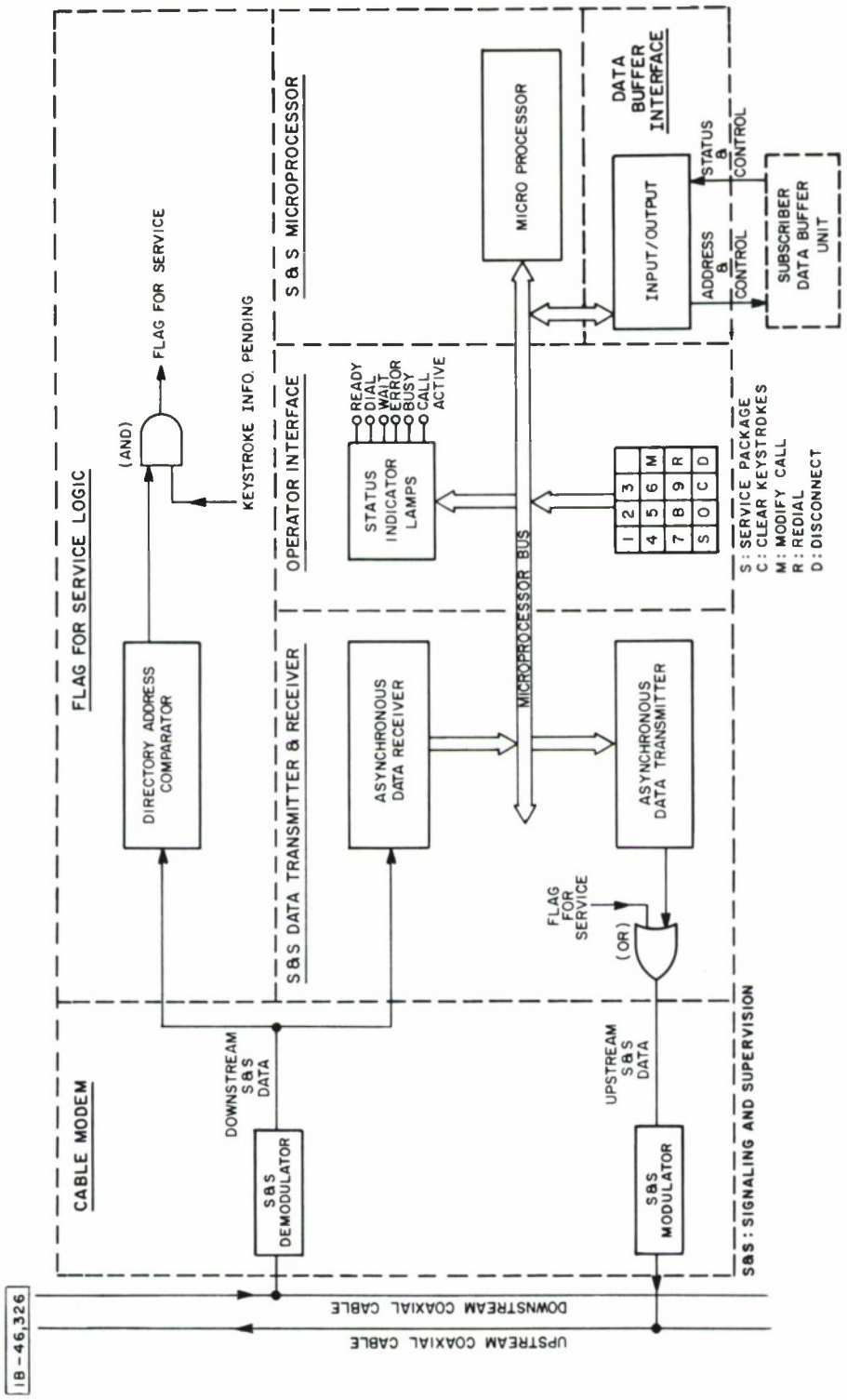

Figure 14 KEYPAD CONTROL UNIT

parallel 4-bit groups, referred to as nibbles, to the microprocessor RAM memory via the microprocessor bus. The microprocessor examines the first 4 nibbles to determine if they contain the Keypad Control Unit's polling address. The four nibbles are equivalent to the 16-bit computer word sent by the PDP-11 Network Control Processor. If a match is found in the 14-bit address field, the last two bits are decoded to determine which control mode applies to the next two words.

When the control mode is 00, the microprocessor interprets these words as an interrogation poll. The microprocessor responds by sending the keystroke/status information via the microprocessor bus structure to the Asynchronous Data Transmitter. The Asynchronous Data Transmitter assembles two 4-bit nibbles into an 8-bit character and transmits them in bit serial mode via the OR gate and modulator interface to the upstream cable.

When the control bits are 01, the microprocessor interprets them as a command poll. The next four characters contain an indirect receiver address and a transmitter address. The microprocessor stores these address words amd retransmits them in 4-bit nibbles to the input/output device shown in the Data Buffer Interface block. The Data Buffer Interface performs the complete equipment interface between the Keypad Control Unit and the Subscriber's Data Buffer Unit that is part of the MIDS digital distribution subsystem (Section 4.3).

When the control bits are 10, the microprocessor interprets them as a command poll with the next four characters containing status light information. The microprocessor sends the appropriate lamp information via the microprocessor bus to the subscriber status lamp driver circuits.

3.6.1 Flag-For-Service Logic

The output of the S&S Demodulator is applied simultaneously to both the Frame Gap Detector and the AND gate input of the Bit Counter (256) as illustrated in Figure 15. After detecting the frame gap at the start of the S&S message, the Frame Gap Detector sends the Frame Sync signal to the Count/Data Steering Flip-Flop. The Frame Sync signal sets the steering Flip-Flop which causes the Count Enable line to go high. If the Power-Is-Up signal is also present, the AND gate of the Bit Counter (256) is enabled, and the counter will commence counting.

Either a Frame sync signal or a Power Clear signal will cause a reset signal to be applied to the Bit Counter (256) and the Group

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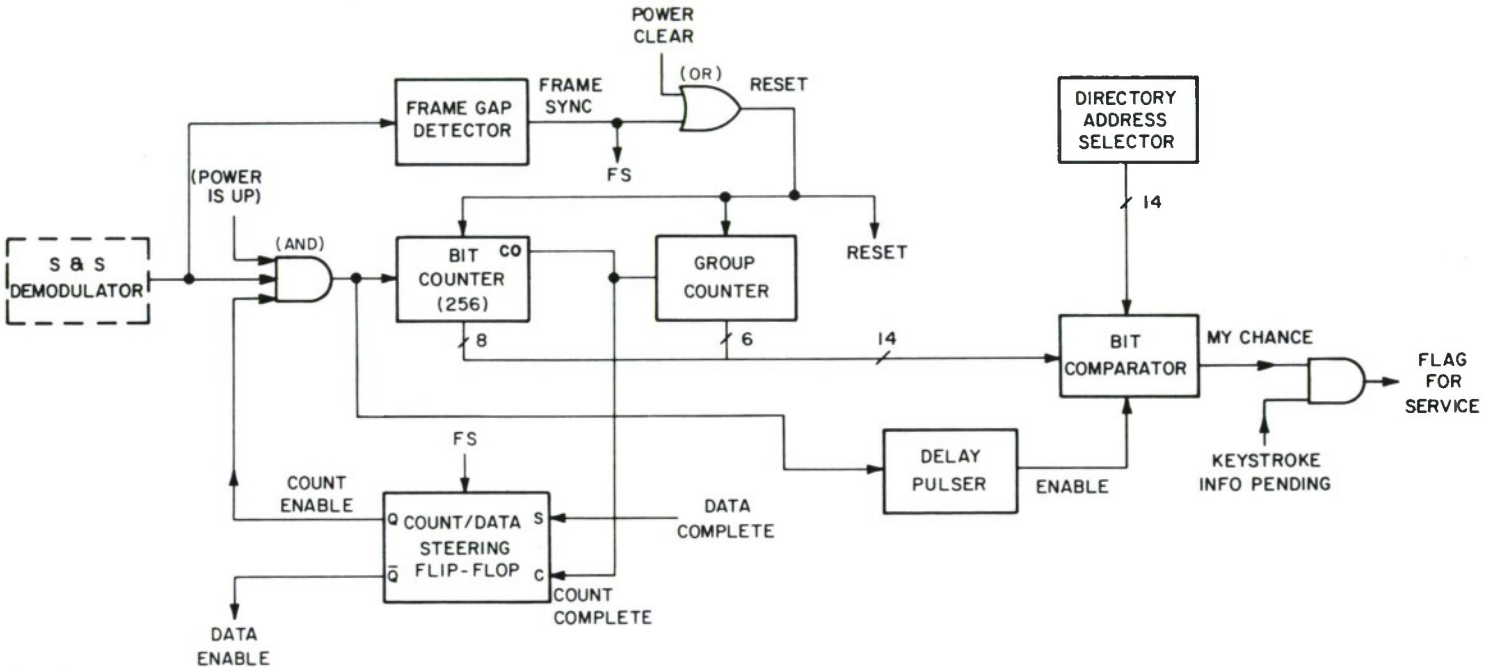


LEGEND

CO: CARRY OUT
FS: FRAME SYNCHRONIZATION
Q : FLIP-FLOP OUTPUT
$\bar{Q}$: COMPLEMENT FLIP-FLOP OUTPUT
S : SET
C : CLEAR
S&S: SIGNALING AND SUPERVISION

SYMBOLS

/N: INDICATES NUMBER OF LINES

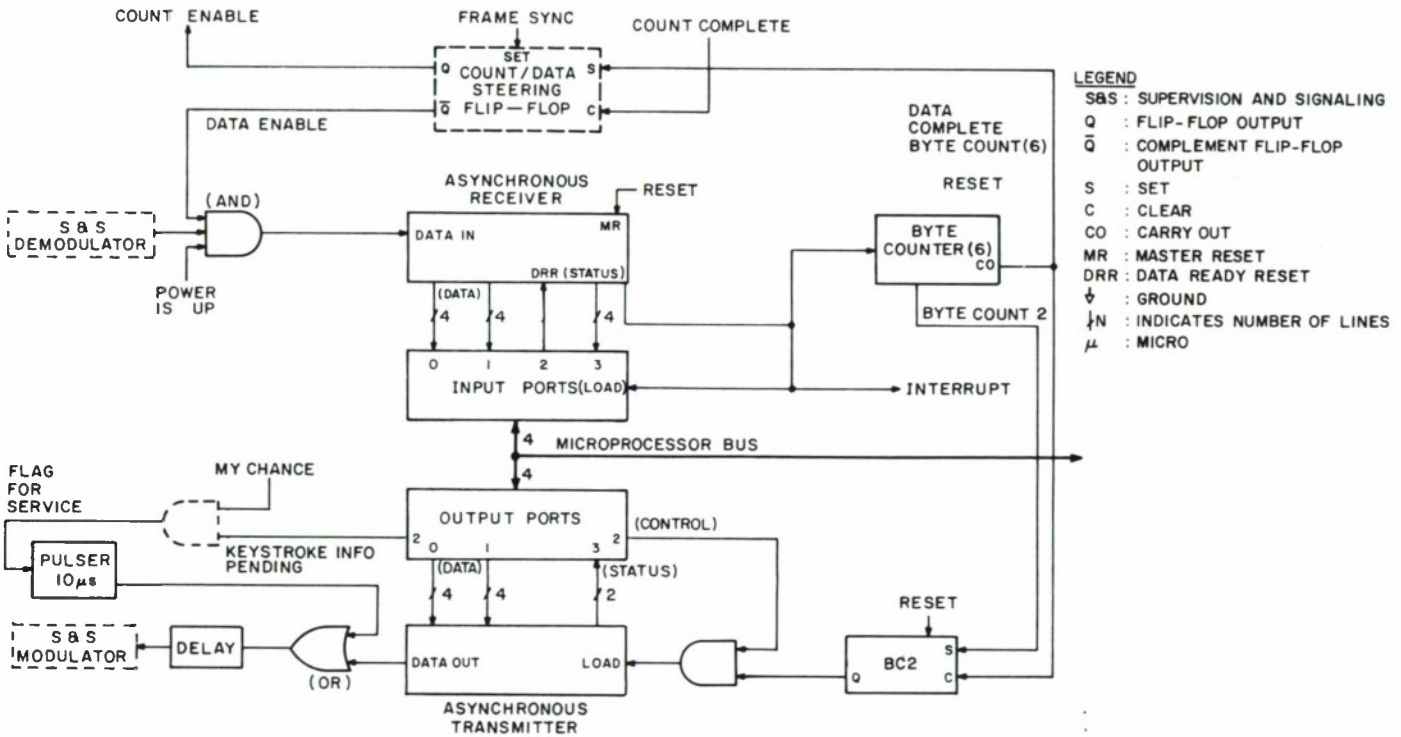
Figure 15 FLAG FOR SERVICE LOGIC

Counter. The reset signal is also available for use elsewhere within the keypad control unit logic. Since there are 64 time groups in one time frame with each group containing 256 bits, a group counter is needed in addition to the bit counter. When the flag-for-service field portion of the time group reaches the 256th bit count, the Bit Counter (256) enables the Carry Out signal which sets the first count in the Group Counter and clears the Count/Data Steering Flip-Flop. In effect the steering Flip-Flop switches off the Count Enable signal thus disabling the Bit Counter (256) and switches on the Data Enable signal. The Data Enable line is routed to the Signaling and Supervision Data Transmitter and Receiver logic circuits.

During the preceding control process the bit count and the group count are being constantly sent to the Bit Comparator. The total bit count during the entire time frame is compared to the count in the Directory Address Selector. When the Bit Comparator finds a match, it causes the signal "My Chance" to occur. If the Keystroke Information Pending signal is being received from the Operator Interface Unit, the Flag-For-Service line becomes active. To prevent the Bit Comparator from accepting spurious states from the Bit Counter (256) and the Group Counter, a delay pulser circuit is used to produce a slight time delay between initially activating the counters and reading their outputs.

3.6.2 Signaling and Supervision Data Receiver and Transmitter

When the bit counter of the flag-for-service logic reaches a count of 256, it sends a Count Complete signal to the Count/Data Steering Flip Flop (Figure 16). The Q′ output of the flip flop sends a Data Enable signal to the AND gate preceding the Asynchronous Receiver. The Asynchronous Receiver has an internal double-buffer register structure. Assuming the power is up, the demodulated S&S signal is able to pass through the AND gate to the Asynchronous Receiver. The Asynchronous Receiver recognizes the first bit as a start bit and shifts the next eight bits into its receiver register. After the stop bit is detected, the contents of the shift register are transferred in bit-parallel form to the second register of the double buffer, that is, the receiver holding register. In addition the parity bit is checked and, if parity is not valid, a signal is placed on the status line. A data ready signal is then generated which performs the following functions:



Figue 16 SIGNALING AND SUPERVISION DATA RECEIVER AND TRANSMITTER

- Sends an interrupt signal to the microprocessor
- Sends a load signal to the Input Port chip of the microprocessor
- Sends a signal to the Byte Counter (6) which advances the byte counter by one

Upon receipt of the load command from the Asynchronous Receiver the Input Port chip of the microprocessor accepts the 8 bits in parallel over its incoming eight data lines. The incoming 8 data lines are divided between ports 0 and 1 with each port servicing four lines. The Input Port chip also reads in the parity and other status through port 3. The microprocessor then sends a data received reset (DRR) signal via port 2 to the Asynchronous Receiver to indicate the completion of the data transfer.

The interrupt signal received by the microprocessor causes an immediate branch to a special location in memory which identifies the new program sequence (called an interrupt handler) to be followed. The microprocessor then sends three successive commands to the Input Port chip. On receipt of the first command the Input Port chip loads the first data nibble in port 0 on the bus. On receipt of the second command it loads the next nibble from port 1. On receipt of the third command it loads the status nibble from port 3. Upon receipt of these three nibbles the microprocessor branches back to its original program and continues its background operations under control of its supervisor program until it is interrupted again.

Each time an incoming character is received the Byte Counter (6) is advanced by a count of one. When the second character is received, the Byte Counter (6) sends a "byte count 2" signal which sets the BC2 flip-flop. The output of the flip-flop is sent to an AND gate which is used as a control element for the Aysnchronous Transmitter. If the microprocessor has sent a keystroke or status message over the microprocessor bus to its Output Port chip, the chip enables the other half of the AND gate through its control line. The enabled AND gate activates a load signal to the Asynchronous Transmitter which then reads the output data in bit-parallel from ports 0 and 1. The Asynchronous Transmitter also has a double-buffer register structure similar to the asynchronous receiver. The register interface in the Output Port chip is called the transmitter holding register and the register interfacing the modulator is called the transmitter register. The Asynchronous Transmitter transfers a character internally in bit-parallel mode

from the transmitter-holding register to the transmitter register. This frees the transmitter-holding register so it is available to accept the next character from the Output Port chip. In the meantime, the Asynchronous Transmitter is sending the character in its transmitter register to the modulator in bit-serial mode. The double buffer feature of the transmitter and receiver is very valuable to the microprocessor. It allows the microprocessor almost one character transmission time to perform other background routines. If the double buffer was not present it would have to act within one bit time whenever characters were being transmitted or received.

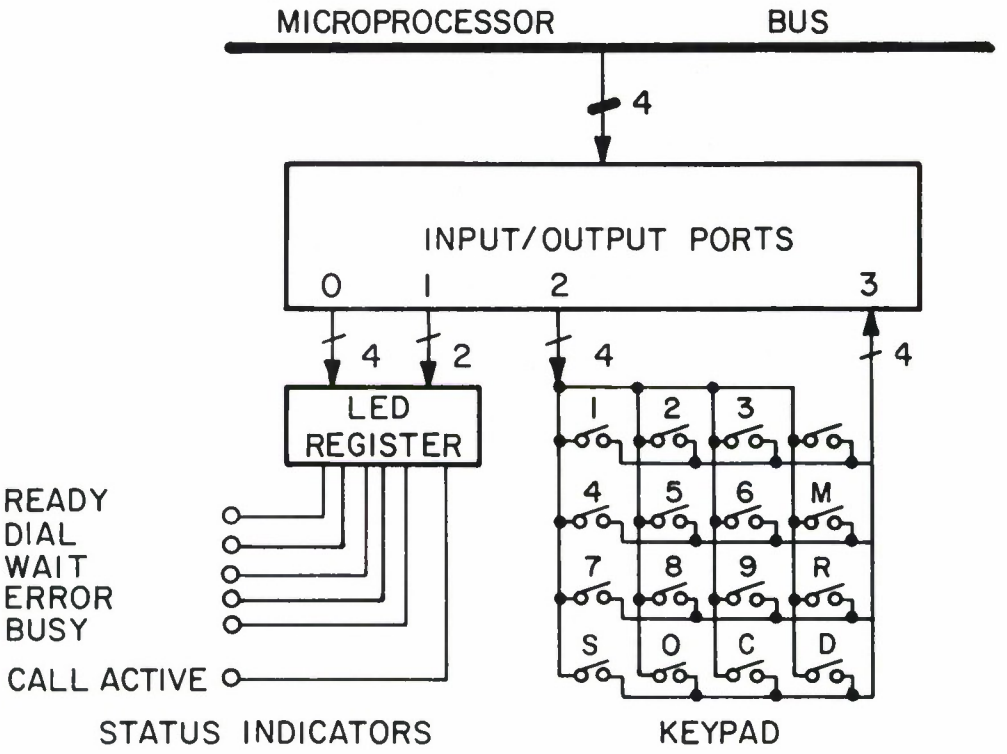
The control cycle is complete when six incoming bytes have been received by the Byte Counter(6). The carry out signal is enabled and applied to the set lead of the Count/Data Steering flip-flop which in turn enables the flag-for-service counting logic for the next time group of the message frame. In addition the carry out signal is sent to the BC2 flip-flop which clears the flip-flop and disables the AND gate control line to the Asynchronous Transmitter.

3.6.3 Operator Interface

The keypad and status indicators are connected to the microprocessor through another Output Port chip as illustrated in Figure 17. Each port services four lines so ports 0 and 1 are used to service the six indicator lamps, leaving two spare lines on Port 1. The keypad is connected via the four outgoing lines of Port 3 and the four incoming status lines of Port 4.

The microprocessor is programmed to scan the keypad as part of its background software routine. Thus the keypad need not send an interrupt signal to the microprocessor as was the case with the asynchronous receiver. The keypad is arranged as an NxM matrix of key switches. In this case both N and M are equal to four. Under program control the first line of the output port is activated. All four input lines to the keypad are read and tested to see if a key has been pressed. The testing uses a special keyboard instruction in the software called KBD. If no key has been pressed, the accumulator of the microprocessor's central processing unit remains at 0000. If a key has been pressed, the accumulator (ACC) indicates the bit position of the key.

By repeating this procedure for each output line in turn the entire keyboard is scanned by the microprocessor. Keystroke characters are stored in the RAM memory and a flag-for-service is invoked. Stored keystrokes are then transmitted to the Network Control Processor upon interrogation polling.



LEGEND

M : MODIFY CALL

R : REDIAL

S : SERVICE PACKAGE

C : CLEAR KEYSTROKES

D : DISCONNECT

LED: LIGHT EMITTING DIODE

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SYMBOL

/ N: INDICATES NUMBER OF LINES

Figure 17 OPERATOR INTERFACE

3.6.4 Signaling and Supervision Microprocessor

The central processing unit (CPU) receives four signals from the clock driver chip as illustrated in Figure 18. The clock driver chip contains a crystal controlled oscillator, clock generation circuitry, and two phase clock driver circuits. The clock driver uses an external crystal. The reset signal is generated whenever power is initially activated. Phase 1 and phase 2 signals provide the basic timing circuits for the entire microcomputer system. The stop signal allows the CPU to execute instructions one at a time. This single step operation provides a convenient means for testing the hardware and programs during the initial design-debugging stage. The control of the stop signal also provides the run/halt feature.

The CPU is a single chip, four-bit parallel MOS central processor. The CPU contains the necessary hardware to accept and process single level interrupts as from the Asynchronous Data Receiver. The CPU generates a synchronization signal which is sent to the various RAM and ROM chips and the peripheral chips in the system. The synchronization signal indicates the beginning of an instruction cycle. The central processing unit connects to a bi-directional data bus called the microprocessor bus. All transfer of address and data communications between the processor and the RAM, ROM, and peripheral chips is handled by way of these four lines.

A RAM memory chip can store 320 bits arranged in 4 registers of twenty 4-bit nibbles. The eighty nibbles of storage are so indicated in the diagram. The RAM memory is used in this application to store received information characters, keystrokes, indirect data buffer addresses, indicator status lamps, etc.

The ROM memory is of the erasable and programmable type and is sometimes called an EPROM. The EPROM is a 256 by 8 bit memory that is equivalent to 256 bytes of program instruction. Each instruction may consist of one or two bytes. The EPROM is packaged in a twenty-four pin, dual-in-line package with a transparent quartz lid. The transparent quartz lid allows the user to expose the chip to ultraviolet light to erase the memory pattern. A new pattern can then be written into the device by a piece of special programming equipment available from a number of manufacturers. This procedure may be repeated as many times as required during the development of the system. A standard Memory Interface chip is used between the EPROMS and the CPU to accommodate up to 16 EPROMS for a total of 4K instruction bytes. The standard memory interface is synchronized to the processor by the sync signal generated by the processor and sent out at the beginning of each instruction cycle. The memory interface chip receives three successive 4-bit nibbles from the

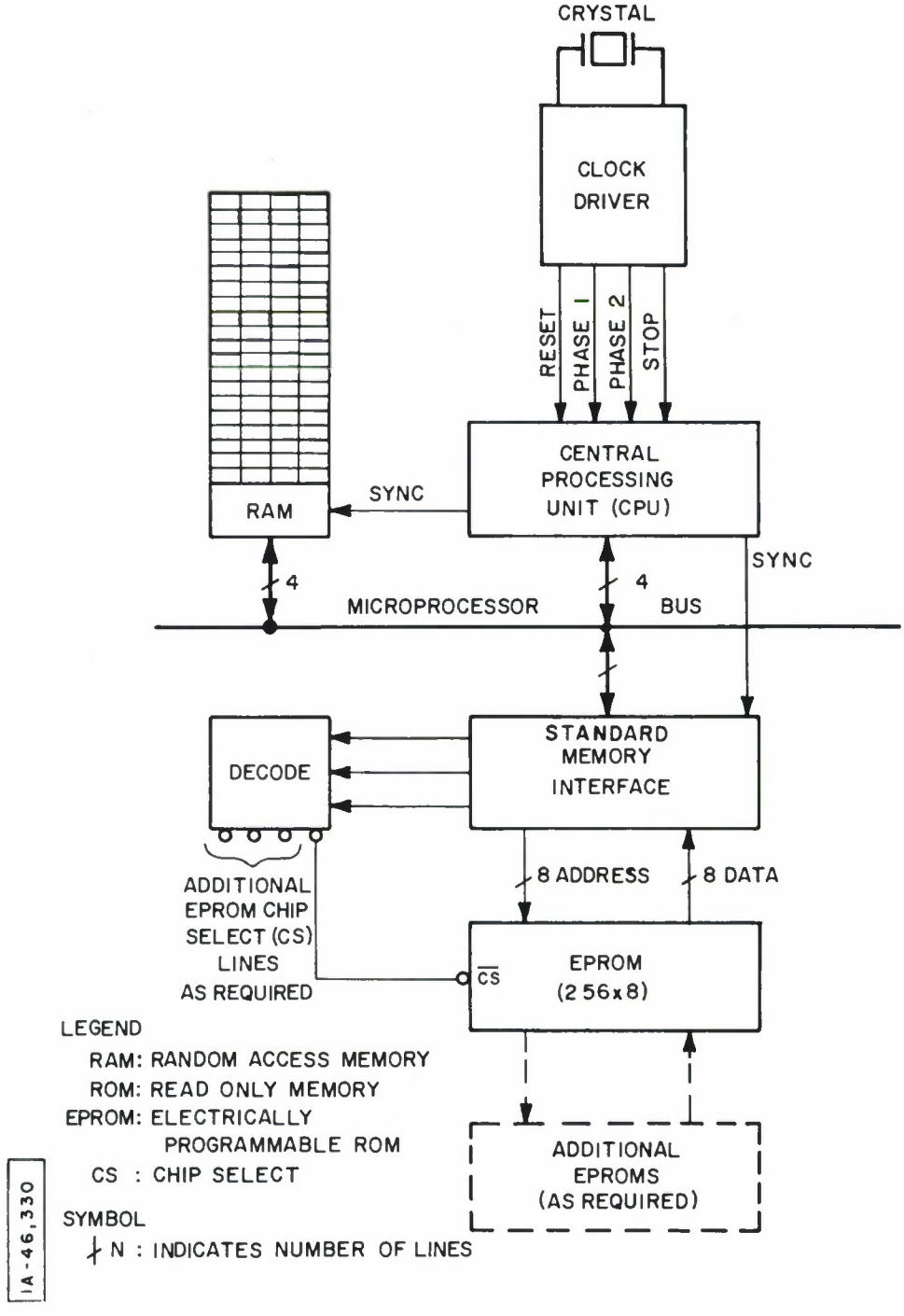


Figure 18 KEYPAD CONTROL UNIT MICROPROCESSOR

central processing unit. It presents these three nibbles in 12-bit parallel form on the 8 address lines and the 4 control lines. The 4 control lines are decoded by the Decode block and one of up to 16 EPROM chips is designated. The designated EPROM decodes the 8 address leads to select one of the 256 8-bit bytes in its memory. The selected byte is then transferred to the Standard Memory Interface via the 8 data lines. The Standard Memory Interface in turn transfers the 8 bits to the CPU as two successive nibbles. It should be noted that the EPROMS contain the operating software program for the microprocessor. They also contain the fixed data used by the microprocessor, whereas, the RAMs contain the variable data that occur during the transactions processed by the CPU.

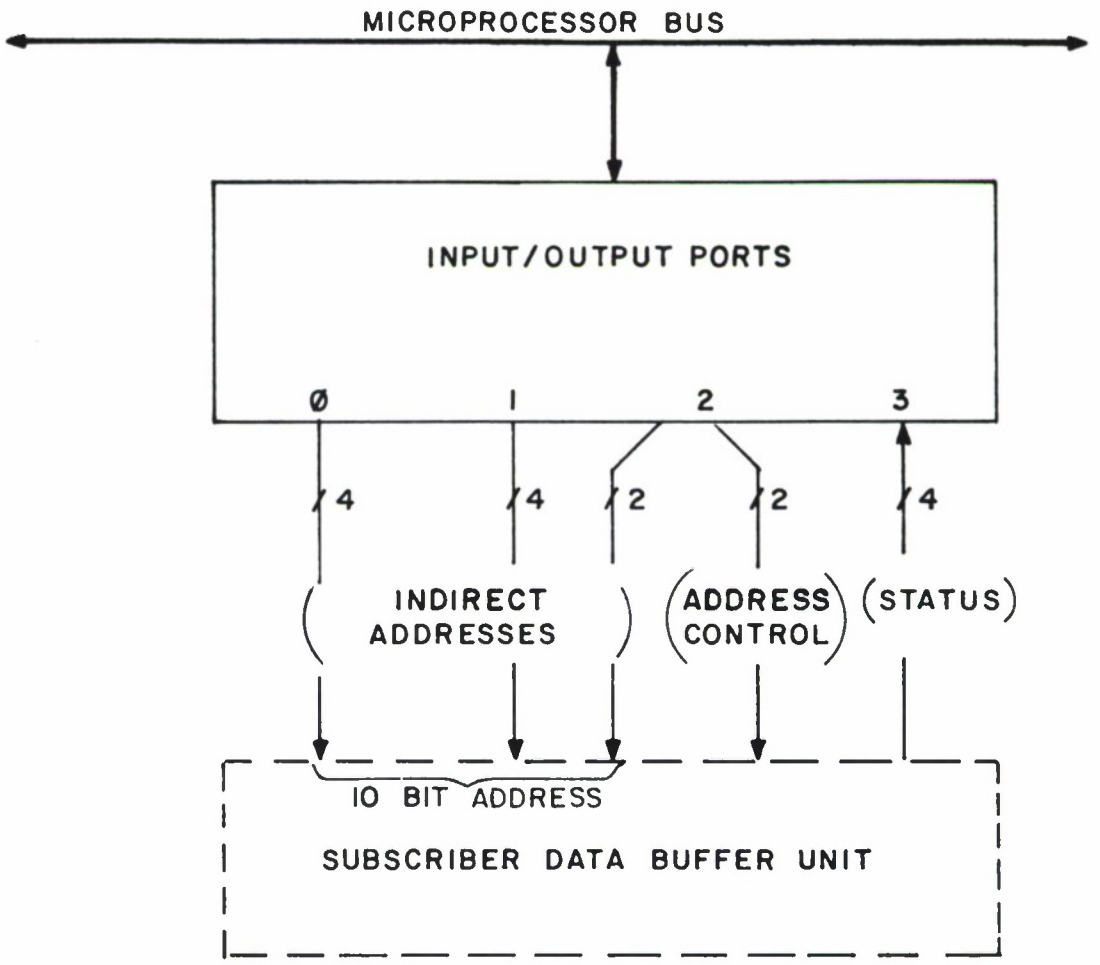
3.6.5 Subscriber Data Buffer Interface

The S&S microprocessor interfaces with the Subscriber Data Buffer Unit through an Input/Output Port chip as illustrated in Figure 19. The Subscriber Data Buffer Unit is part of the MIDS Digital Data Distribution subsystem. When a subscriber requests data distribution service through his keypad, the Network Control Processor sends two indirect addresses to the Keypad Control Unit for use by the Subscriber Data Buffer Unit. These indirect addresses are not permanently assigned to any particular user, and therefore vary from connection to connection. One of the indirect addresses is used by the subscriber unit for receiving its messages while the other indirect address is used for transmitting its data to the destination terminal. The two addresses permit full or half-duplex transmission. Ten of the lines between the Input/Output Port chip and the Subscriber Data Buffer Unit are assigned to transferring the indirect address information in bit-parallel form. The remaining lines are devoted to terminal status input.

As part of its normal software routine, the microprocessor continuously monitors the status of the Subscriber Data Buffer Unit. Therefore, an interrupt lead is not necessary from the Subscriber Data Buffer Unit to the microprocessor.

3.7 KEYPAD S&S CONTROL UNIT MODEM

The Keypad S&S Control Unit Modem provides the interface between the RF signals on the S&S channel of the coaxial cables and the digital DC-level signals within the Keypad Control Unit. It also contains a divider circuit for generating timing signals for the Keypad Control Unit's logic circuits.



SYMBOLS

/N INDICATES NUMBER OF LINES

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Figure 19 SUBSCRIBER DATA BUFFER INTERFACE

The modem has the unique feature of using a phase-locked-loop detector circuit in the demodulator section. The circuit contains a phase lock loop and a synchronous AM detector to both regenerate the 16 MHz carrier signal and to detect the S&S data stream. Since all keypad control unit modems working into the upstream cable are generating precisely the same frequency as is received on the downstream cable, the detection of these modulated signals by the S&S channel controller modem is simplified.

A block-diagram representation of the main components of the modem is contained in Figure 20. The carrier frequency used on the downstream cable and the upstream cable is 16 megaHertz. The carrier on the downstream cable is amplitude modulated by the S&S Channel Controller with the Mark (1) condition being represented by 50% carrier level and the Space (0) condition by 100% carrier level. The condition of some carrier signal from the channel controller modem always being on the cable is necessary so that the phase lock loop circuit in the Keypad Control Unit may stay locked regardless of whether a 1 or a 0 is being transmitted. The downstream cable frequency is applied to a tuned RF amplifier that contains a band-pass filter centered at 16 megaHertz. The output of the amplifier is used to drive the phase lock-loop-detector circuit. The Phase Lock Loop Detector supplies data to the Keypad Control Unit through a Line Driver circuit. In addition, it provides a precise 16 megaHertz to a tuned amplifier driver circuit.

The Phase Lock Loop Detector contains a voltage-controlled oscillator, a phase detector and an error amplifier circuit configured in a classical negative feedback mode. When the circuit is first activated, the voltage-controlled oscillator is in a free-running state and is generating a frequency close-to but not exactly the same as the downstream cable frequency. The phase-detector portion of the circuit detects this difference which is amplified and applied to the voltage-controlled oscillator. The voltage-controlled oscillator is driven in the direction of producing a frequency the same as the downstream cable. As the frequencies approach each other the error signal gets smaller and smaller until the frequencies are exactly the same and only a slight difference in phase exists between the incoming frequency and the frequency produced by the voltage-controlled oscillator. This slight difference is necessary in order to produce the error signal which is amplified to continually drive the voltage-controlled oscillator in the correct direction.

For convenience the modem also includes a "divide by 48" circuit to produce a 333 kiloHertz clock signal for the asynchronous data receiver portion of the keypad control unit. This frequency is "16

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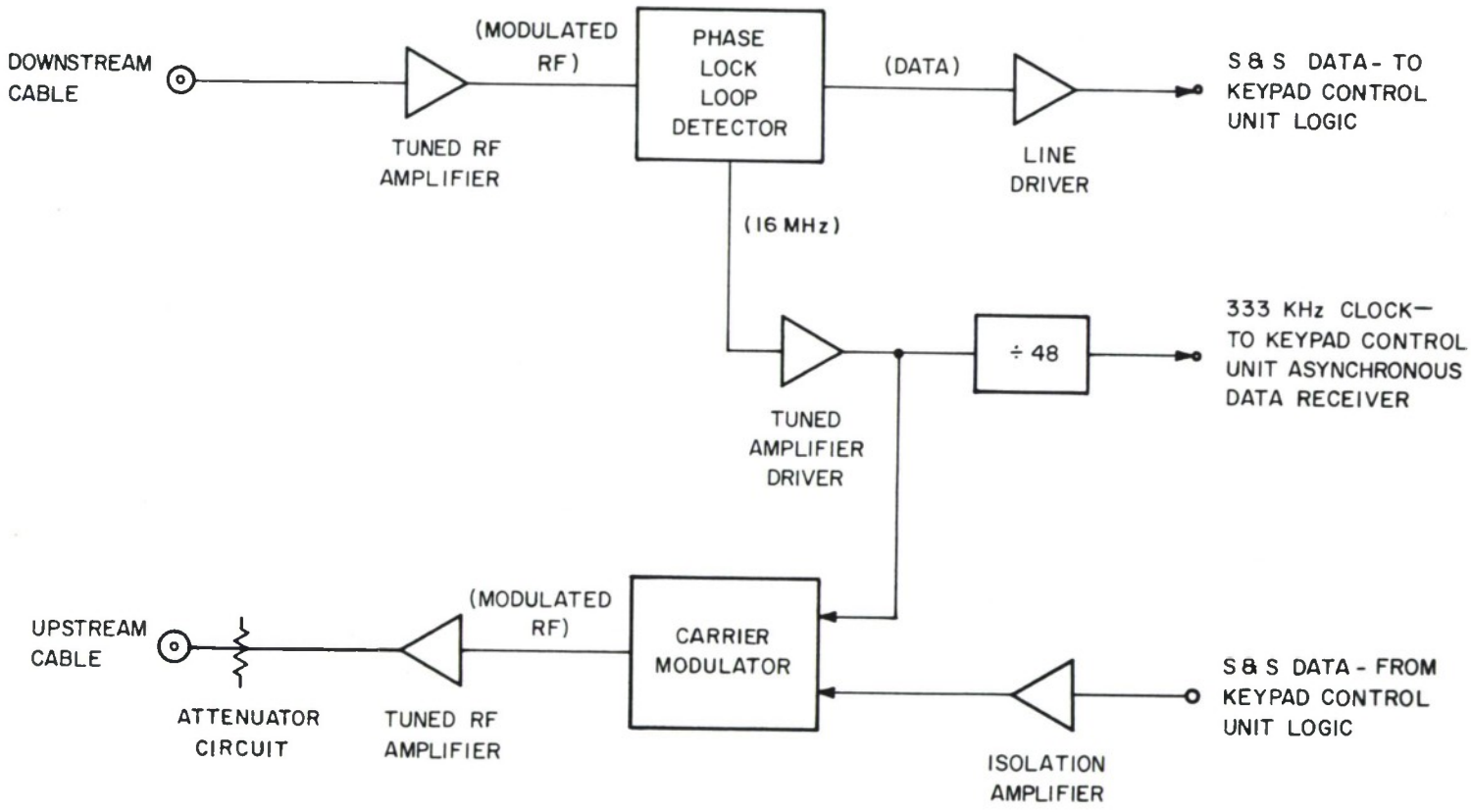

Figure 20 KEYPAD CONTROL UNIT MODEM

times" the data transmission rate used on the upstream cable. The 16 times is a feature of the so called universal asynchronous receiver transmitter (UART) chip marketed by a number of chip manufacturers.

The 16 megaHertz signal is also supplied to the carrier modulator portion of the modem. The digital data signal from the keypad control unit logic is fed to the same carrier modulator circuit through an isolation amplifier. The output of the carrier modulator is the modulated RF which is amplified by a tuned RF amplifier for driving the upstream cable. An attenuator circuit containing replaceable resistor "pads" is used to provide precise voltage levels on the cable to minimize cross talk into other channels. The modulator Mark condition is represented by zero carrier and the Space condition by 100% carrier being applied to the cable. The Mark condition is the OFF condition. It is necessary that each Keypad transmitter be off when it doesn't have any upstream message so that it doesn't interfere with other Keypad modems transmitting during their poll responses and to prevent noise accumulation on the upstream cable.

The modem is required to transmit at 46 dbmv (200 millivolts RMS) and receive over the dynamic range of 0 to 20 dbmv (1 mv to 10 mv).

SECTION IV

DIGITAL DATA DISTRIBUTION SUBSYSTEM

4.1 GENERAL

The Digital Data Distribution Subsystem performs the function of transmitting and distributing data messages between the various subscriber devices attached to the cable. As indicated in Figure 1 data distribution over the cable is managed by the Data Channel Controller and each subscriber terminal is connected to the cable via a Subscriber Data Buffer Unit. Large computers acting as host processors are connected to the cable via a Multiport Data Buffer Unit. Simultaneous communication between 64 subscriber terminals and the host processor is possible with a single multiport data buffer unit.

The subscriber receives data service after making a service request via his Signaling and Supervision Keypad Control Unit. The request is transmitted over the S&S control channel of the cable. The S&S Network Control Processor determines if the request is valid and the necessary equipments available. If so, it sends a set of indirect addresses to the Keypad Control Unit. The Keypad Control Unit is collocated with the Subscriber Data Buffer Unit and passes the indirect addresses directly to it. The Subscriber Data Buffer Unit uses these addresses for transmitting and receiving messages over the data distribution channel.

A form of polled, time-division multiplexing is used for transmission over the data distribution channel. Transmission is at the rate of 2.25 megabits per second using phase modulation of a 13.5 megaHertz carrier. Individual terminals transmit at an average standard rate of 600 bps. Up to 1024 terminals may be accommodated simultaneously.

Terminals requiring higher speeds than 600 bps are automatically switched to a higher polling rate by the channel controller to permit terminal operating speeds to 19.2 kbps.

4.2 DATA DISTRIBUTION SUBSYSTEM TIMING AND MESSAGE FORMAT

The polling sequence and message format used by the digital data subsystem channel controller is illustrated in Figure 21. The polling sequence alternates between low-speed service and high-speed service. The low speed addresses are assigned sequentially, and the high speed addresses are assigned explicitly in accordance with the

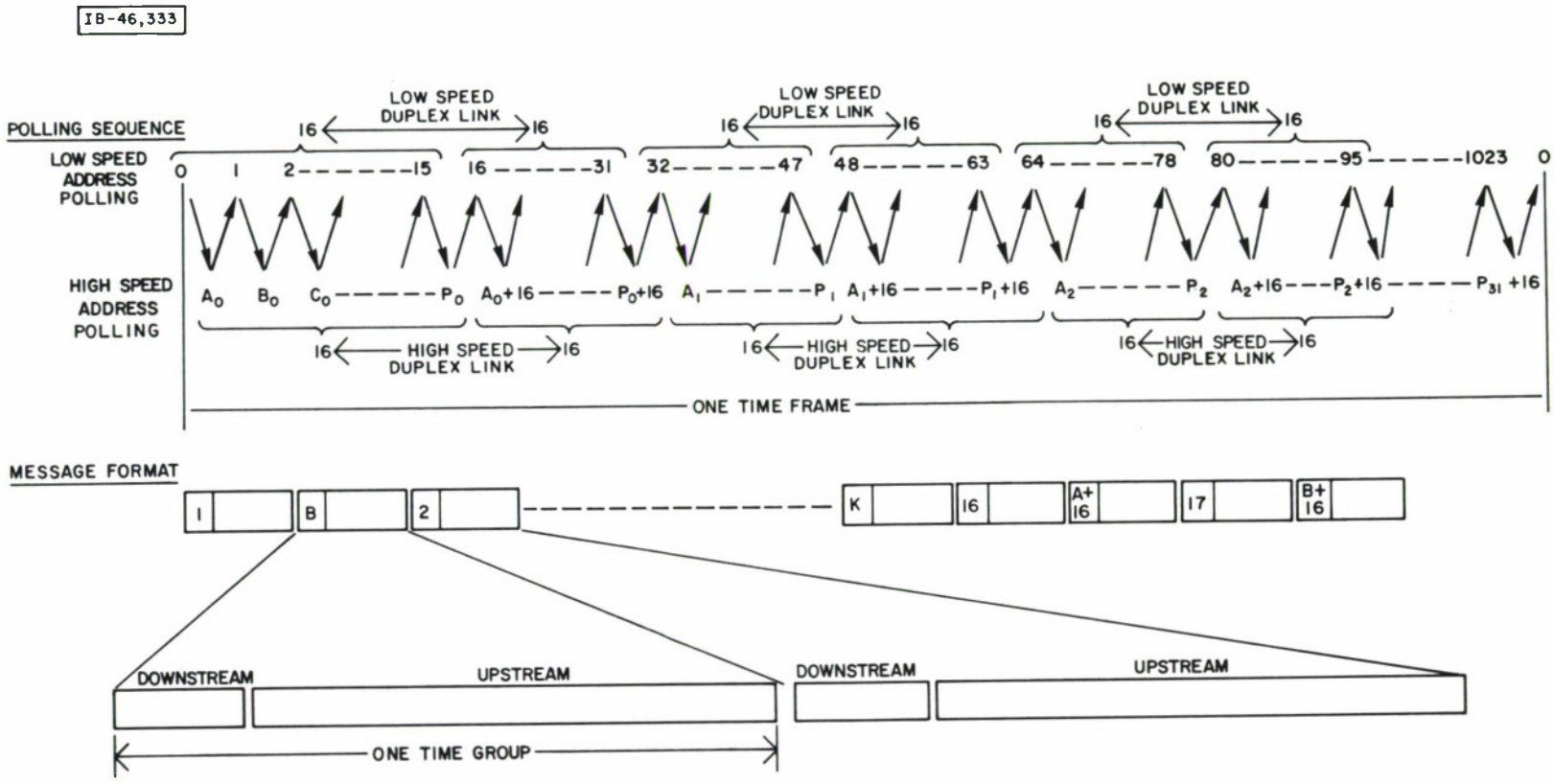

Figure 21 DATA DISTRIBUTION SUBSYSTEM POLLING AND TIMING

requests for service. For ease of representation low-speed addresses are shown as starting at 0 and extending through 1023, for a total of 1024 addresses. The high-speed addresses are represented symbolically by the letters A through P for a total of 16 addresses.The subscripts indicate successive polling cycles within the same time frame. Once a terminal is assigned to high-speed service, it receives high-speed polls during an entire time frame. The channel controller's microprocessor determines which low-speed addresses are to be assigned high-speed service in the next time frame. The protocol which handles this assignment is such as to give all requestors a turn at high speed service. This feature is the heart of the system's automatically adaptive data rate capability.

Since the Data Channel Controller alternately issues low-speed and high-speed addresses, a total of 2,048 addresses are sent during one time frame. In setting up the data paths full-duplex links are always established, therefore the 1,024 low-speed addresses permit 512 full-duplex low-speed links. For reasons of implementation, it was convenient to group low-speed service addresses into groups of 16 pairs. As indicated in the diagram, the first 16 addresses in the low-speed polling sequence are duplex-connected to the next 16 addresses. This creates commonality of duplex address assignments between high speed and low speed service, wherein the addresses of duplex pairs are always separated by the numeric 16.

A portion of the 2048 data transmission time groups in a time frame is indicated by the middle level of Figure 21. The bottom level of the diagram shows an exploded view of two of these time groups. The first time group contains a high-speed polling address and the next time group contains a low-speed polling address as indicated by the letter B and the number 2 respectively. The channel controller sends two synchronization bits, followed by the "B" address which is followed by a parity bit. The remainder of the time in the time group is allowed for the terminal to respond to the downstream polling address.

The message format and bit assignments contained in a time group are indicated in Figure 22. The first word contains the polling address, that is the address of the terminal that wants to transmit. The low-order ten bits of the word are assigned to represent one of the 1024 addresses. The high-order six bits of the word, that is bits 10 through 15, are unassigned and available for future use. The second word contains the address of the receiver terminal, that is the terminal which is to receive the message being sent by the transmitting terminal. The low-order ten bits are assigned to the receiver address. The high-order six bits are control bits. Bits

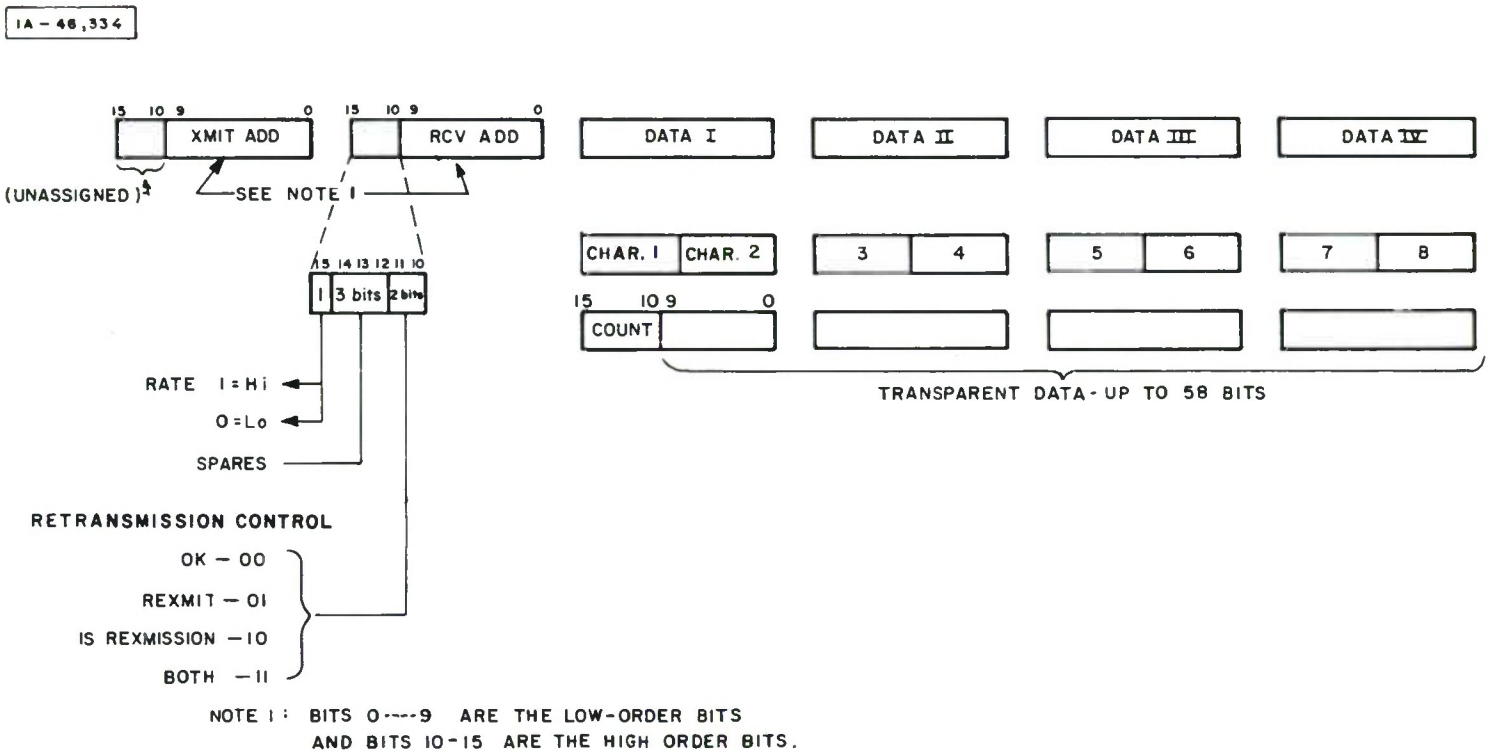

Figure 22 DATA SUBSYSTEM MESSAGE FORMAT

10 and 11 are for transmission control. If the receiving terminal receives a message with bad parity or wants to delay receiving new data, it can request a retransmission from the transmitting terminal by returning a message with the control bits set to 0,1. When the transmitting terminal decodes the control bits, it retransmits the message and sets the control bits to 1,0. Since the digital data subsystem always provides full-duplex connections, the possibility exists that both bits may be set to 1. The terminal sending the message with both control bits set to 1 is indicating that it is retransmitting a message but that it also wants a retransmission from the other terminal. If none of these conditions prevail, the control bits are set to 0,0.

Bit 15 is used as a request-for-high-speed service indicator. When bit 15 is set to 1, the Data Channel Controller will store that terminal's address in a high-speed address queue. The remaining control bits, that is bits 12, 13, and 14 are spares and are available for future use.

The remaining four words of the digital data message are used for transmitting the data information portion of the message. Since data terminal transmission is usually character oriented, each data word may contain two characters with the four data words transmitting eight characters of information. A second mode of transmission is also available. This mode corresponds to a "transparent data" operation. If a terminal device does not transmit in 8-bit character blocks, it may transmit any block length up to 58 bits. The number of bits contained in the block is indicated by Count Bits 10-15 contained in the DATA I word.

Each message time group contains 104 bits. The bit count and pulse time corresponding to the various functions of the bits is indicated in Figure 23. The states indicated by the state counter are also shown for each group of functional bit(s). The bit count is designated by pulse time 1 through 104. The quantity of bits assigned to a particular function appears above the pulse time in the diagram. The functions include the following:

- Message Synchronization
- Polling (Transmitter) Address
- Polling (Transmitter) Address Parity
- Control/Receiver Address
- Control/Receiver Address Parity
- Data Word I
- Data Word I Parity
- Data Word II
- Data Word II Parity

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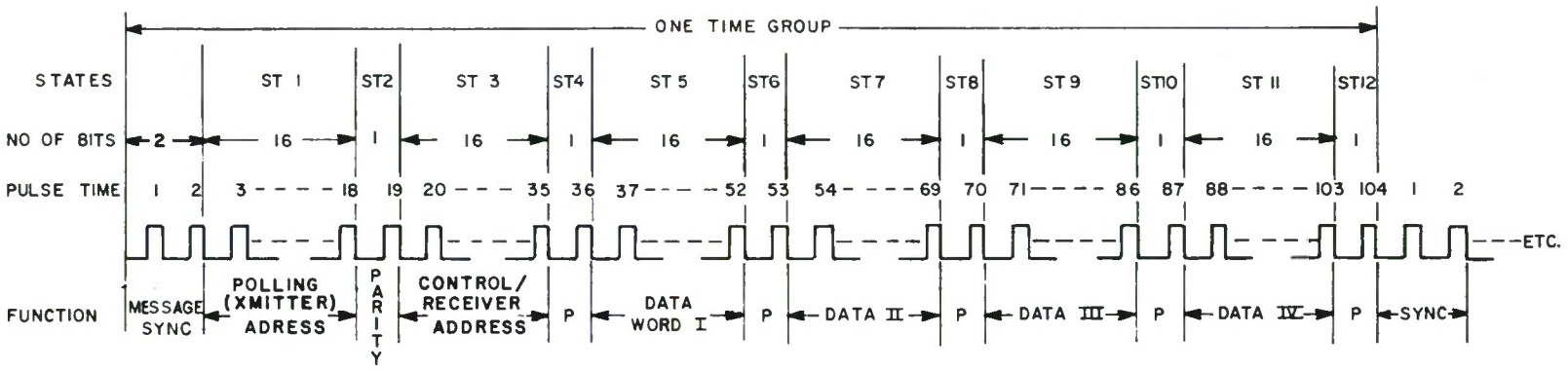

Figure 23. DATA TRANSMISSION TIME GROUP

- o Data Word III
- o Data Word III Parity
- o Data Word IV
- o Data Word IV Parity

States 1 through 12 are also indicated above the functional bit groupings. The state counter sends a State 1 signal during the Polling (Transmitter) Address time, a State 2 signal during the Polling (Transmitter) Address Parity time, etc. The State Counter operation and its control are described in more detail in succeeding sections.

4.3 DATA DISTRIBUTION SUBSYSTEM CHANNEL CONTROLLER

The data distribution subsystem channel controller generates the polling addresses used for low and high speed service and transmits them to all terminal devices via the downstream cable. The polls provide the synchronization and control necessary for transmission of digital data messages on the upstream cable from a large number of terminals. The controller then retransmits these messages onto the downstream cable.

A simplified representation of the data distribution subsystem is shown in Figure 24. The diagram is divided into four functional blocks as follows:

- o Timing Circuits
- o Low-speed and high-speed address poller
- o Request for high-speed service circuitry
- o Microprocessor
- o Input/Output buffer

The Timing Circuits block provides the "clock" signals required to keep the logic circuits within the channel controller synchronized. The Low-speed and High-speed Address Poller block contains a low-speed address poller buffer and a high-speed address poller buffer. Control circuits "toggle" back and forth between these two buffers and transmit the polling addresses via the modulator on the downstream cable. The Request For High-speed Service block is used to examine the messages coming from the terminals. If the message contains a high-speed service control bit set to 1, that address is stored in a buffer called the High-speed Address Request Queue. Whenever the queue receives an address, it sets a Ready "flag" for the microprocessor. The microprocessor retrieves the address and stores it in a high-speed address table within the microprocessor memory. Once every polling cycle the microprocessor loads the high-speed address table into the High-Speed Address Poller. The input/output buffer receives the data from the upstream cable and stores it for transmission on the downstream cable during the next time group.

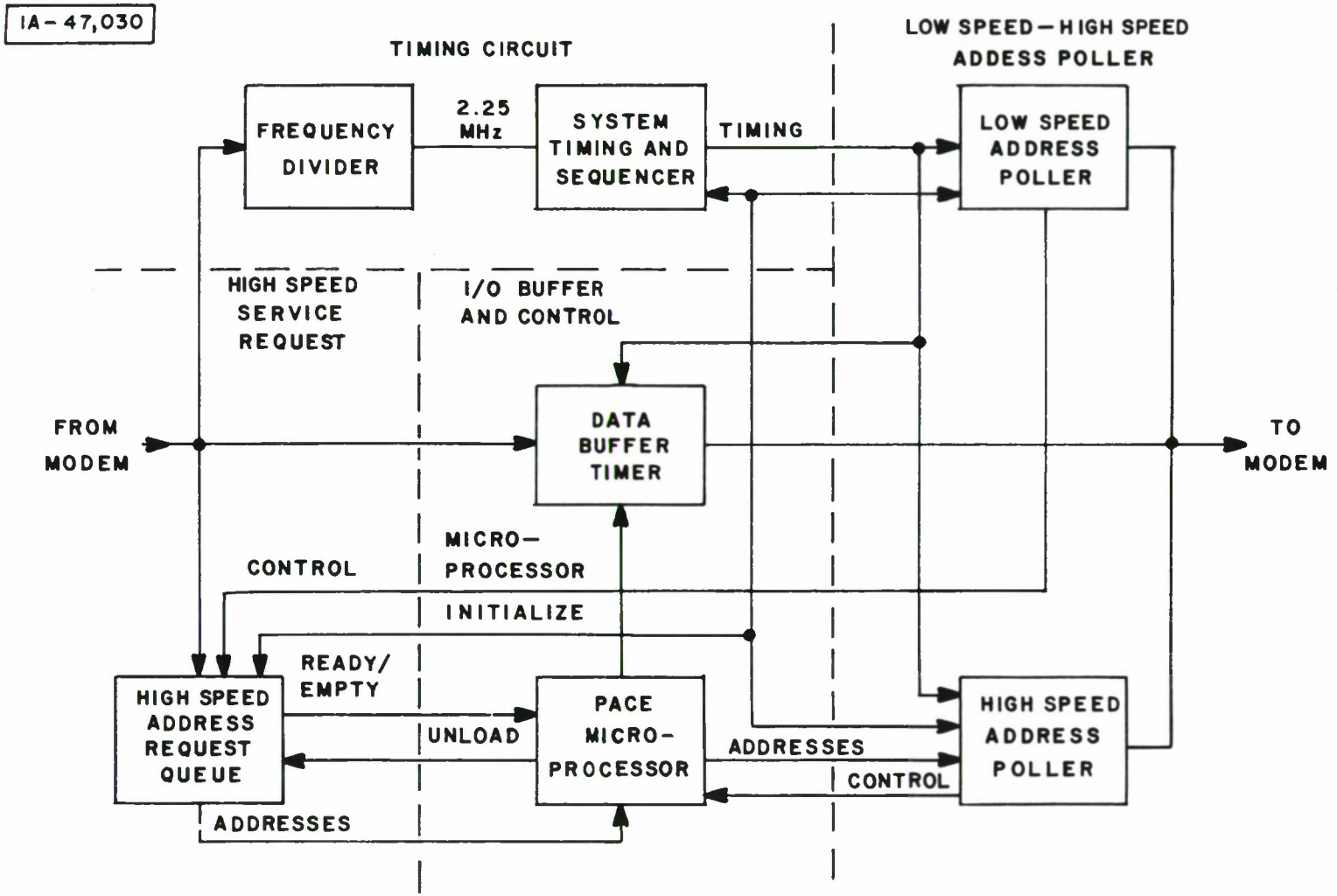

Figure 24. DATA DISTRIBUTION SUBSYSTEM CHANNEL CONTROLLER

4.3.1 Data Channel Controller Timing Circuits

The functional blocks performing the various timing functions are indicated in Figure 25. A stable timing reference is provided by a crystal-controlled oscillator that is part of the modem described in Section 4.5. The 13.5 megaHertz output signal is applied to a "divide-by-6" circuit to produce a frequency equal to 2.25 megaHertz.

The Time Base Counter Modulo 104 refers to the fact that there are 104 bits in a time group as previously identified in Figure 23. The counter is initialized by the microprocessor immediately after power is applied to the system. The counter produces signals that enable the generation of the message sync time slots, the data time slots and the parity time slots. A state counter is used to generate the 12 states indicated in Figure 23. The state counter signals synchronize the logic circuits as indicated in succeeding logic-circuit diagrams. Whenever the message sync time slot appears, the state counter is pre-set to emit the State 1 signal. The generation by the base counter of either a data time slot signal or a parity time slot signal causes the state counter to advance by 1. When the time base counter completes the count of 104, it sends a signal to the Low-Speed Address Poller. The low speed poller contains an eleven stage counter. The low order bit determines if a low or high speed poll is to be performed. The remaining 10 bits are the low speed polling address.

4.3.2 Low-speed and High-speed Address Poller

The logic circuits for the low-speed and high-speed address pollers are illustrated in Figure 26. The low-speed address poller circuits are shown on the left side of the diagram and the high-speed address poller is on the right side. Since the low-speed addresses simply proceed from 0 to 1023, a 10-stage counter is sufficient to generate the low-speed addresses. However, as noted above, an 11-stage counter is used so that the first stage may be used as a toggle for the Lo/Hi Readout Control circuit that controls the alternate sending of low-speed and high-speed addresses. The 10 bits containing the low-speed address are transferred in bit-parallel mode from the counter to a parallel-to-serial shift register. The output of the shift register applies the 10-bit address in bit-serial mode through the gating circuits to the modulator for transmission on the downstream cable. At the appropriate time between transmissions the Counter receives an ADD+1 signal from the Timing Circuits which causes it to increment the low-speed address count by one.

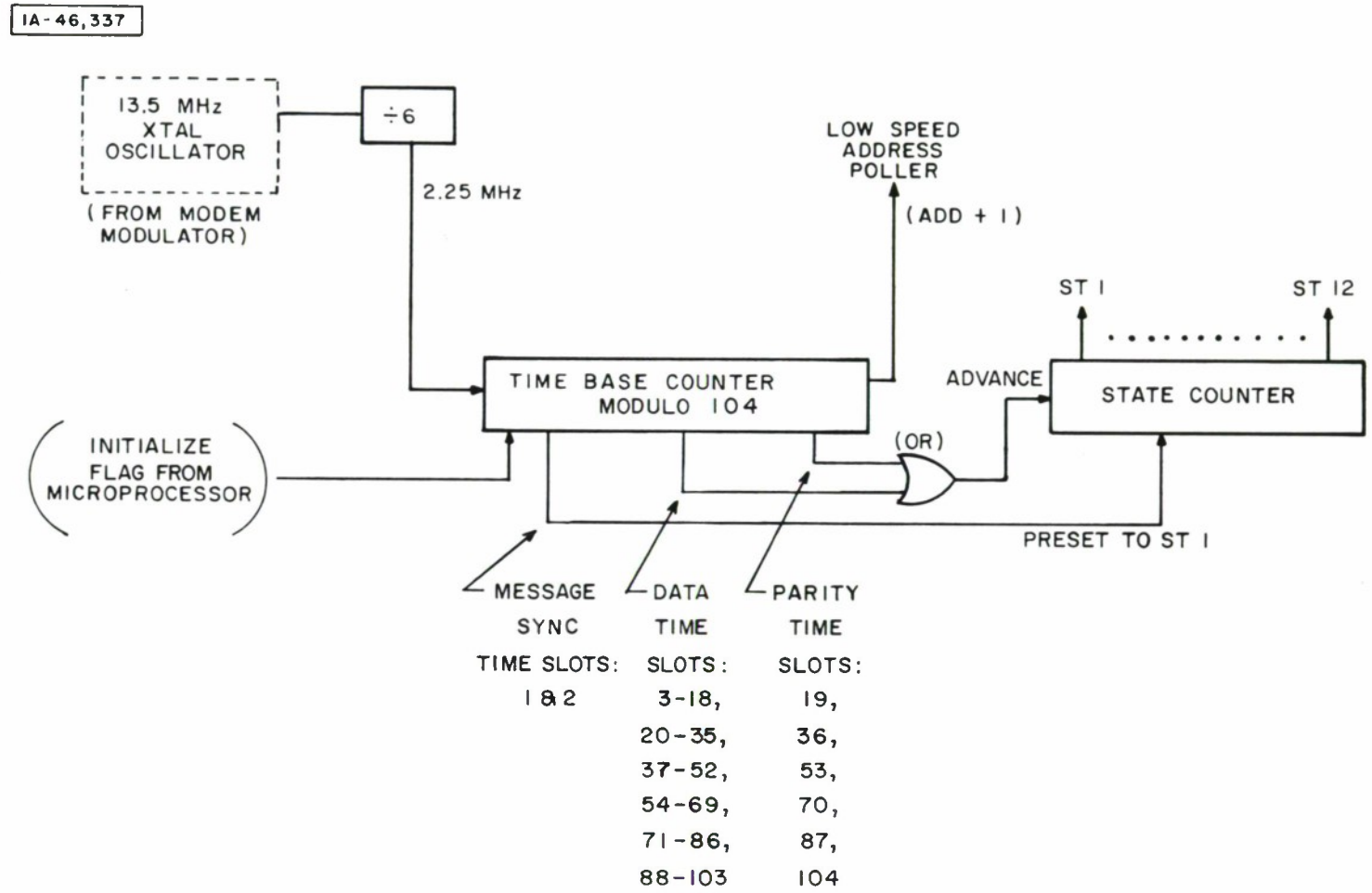

Figure 25 DATA CHANNEL CONTROLLER TIMING CIRCUITS

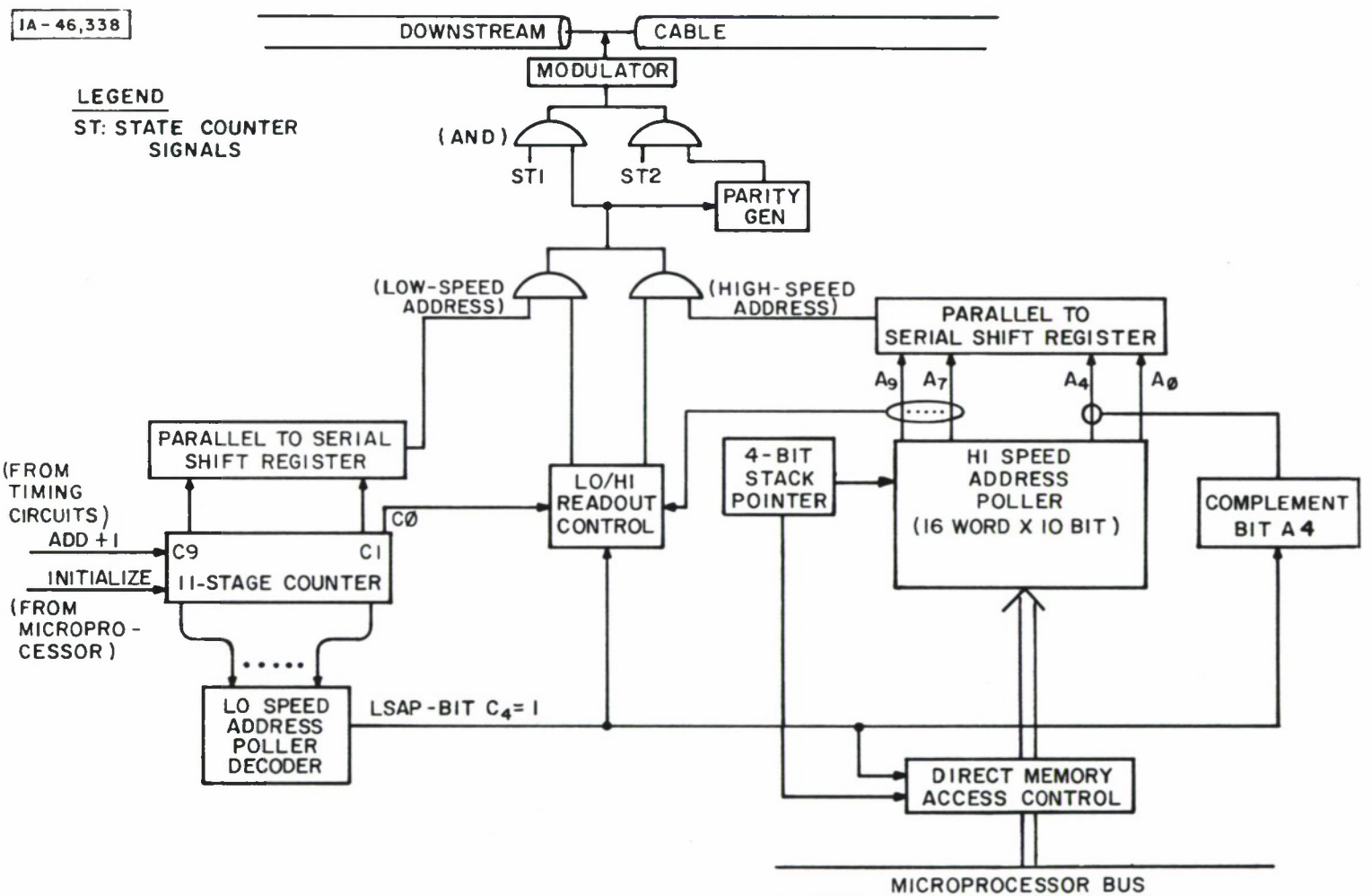

Figure 26 LOW SPEED AND HIGH SPEED ADDRESS POLLER

The High-Speed Address Poller has 16 words stored in its buffer. Each word contains an address to be sent on the downstream cable. The High-Speed Address Poller receives these 16 words from the microprocessor via a direct memory access control technique. The High-Speed Address Poller sends a total of 32 addresses downstream. The second group of 16 addresses is offset from the first group simply by the numeric 16; therefore, only a 16 word buffer is required by the poller. It receives a logic control signal from the low-speed address poller decoder which indicates when to add 16 to the addresses in its table. It performs the Add 16 function by complementing the fifth bit in the output that is sent to the Parallel-To-Serial Shift Register. The High-Speed Address Poller uses a 4-bit stack pointer to indicate to the Direct Memory Access Control circuit that the high-speed addressing polling is complete. This signal is gated with the Low-Speed Address Poller Decoder control signal to set up the next direct memory access to the microprocessor.

For each 16 bits transmitted a 17th bit is sent for parity-checking purposes. The 16 bits sent to the downstream cable are also sent to the Parity Generator. The Parity Generator examines the 16 bits to determine whether they contain an even or odd number of 1's. If they contain an even number of 1's, the Parity Generator places a 1 in the 17th bit position. That is the Parity Generator provides odd parity during State Counter 2 time.

4.3.3 Request for High-Speed Service

The logic circuits within the Request for High-Speed Service block are indicated in Figure 27. As each incoming message is received and demodulated, bit 15 of the Control/Receiver Address word is examined to determine if it is set to 1. If so, it is detected by the High-Rate Bit Detector circuit which enables the AND gate during State Counter 3 time. A signal must also be present indicating that the low-speed poller is active. This insures that a high speed poll cannot set up high speed service, which could result in polls occurring too close together. (This condition is described and explained further in Section 4.2.5, Microprocessor Software Programs.) These conditions permit the address to be passed through the AND gate to the Serial to Parallel Shift Register. The addresses are transferred from the Shift Register to a first-in/first-out (FIFO) buffer called the High-Speed Address Service Queue. Whenever the FIFO buffer receives an address, it sends a Ready signal to the microprocessor. It stores the addresses successively until it receives an Unload signal from the microprocessor. The FIFO buffer has storage capacity for storing 40 words x 10 bits wide.

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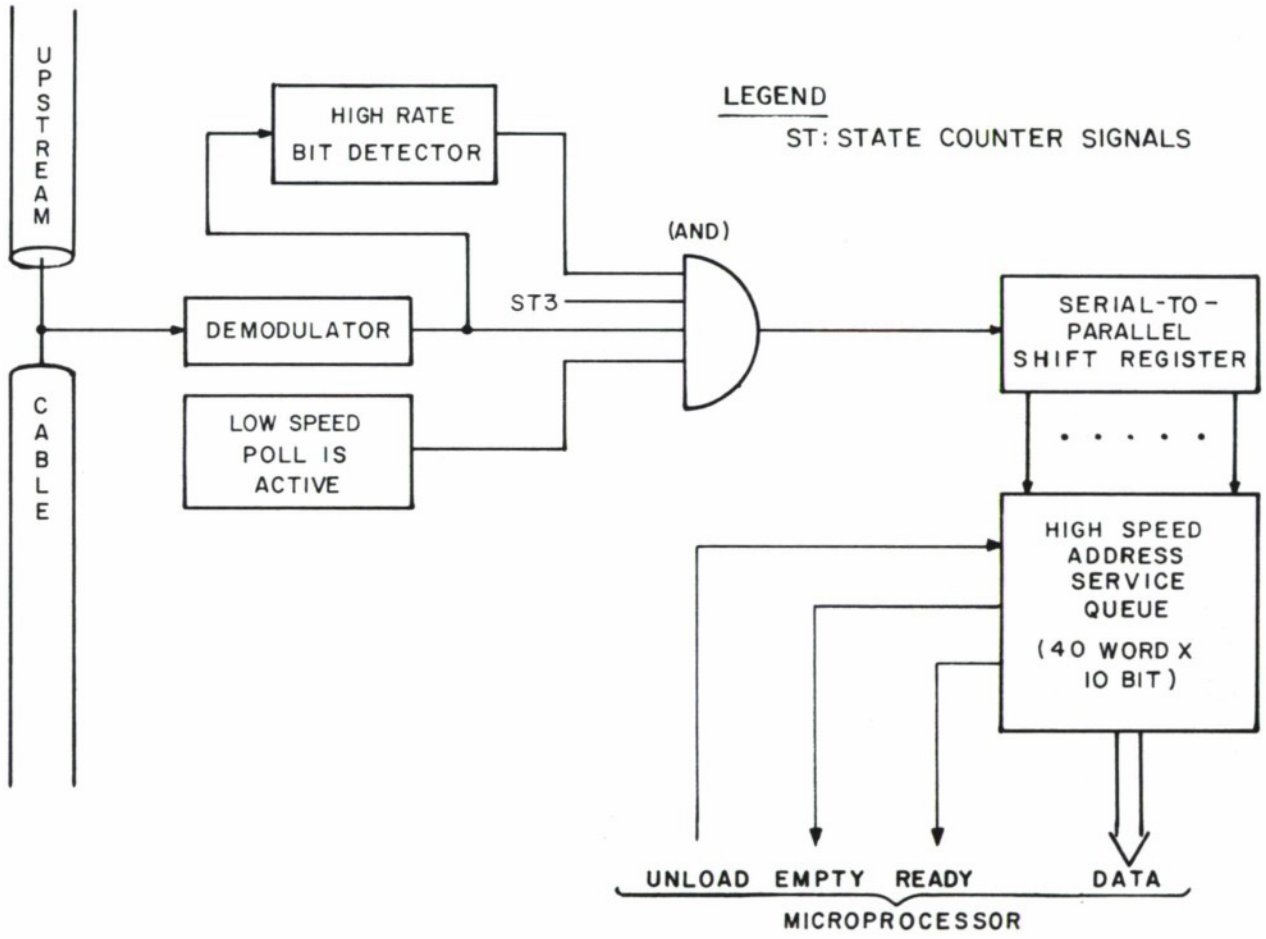

Figure 27 REQUEST FOR HIGH SPEED SERVICE

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LEGEND
PROM : PROGRAMMABLE READ ONLY MEMORY
RAM : RANDOM ACCESS MEMORY
DMA : DIRECT MEMORY ACCESS

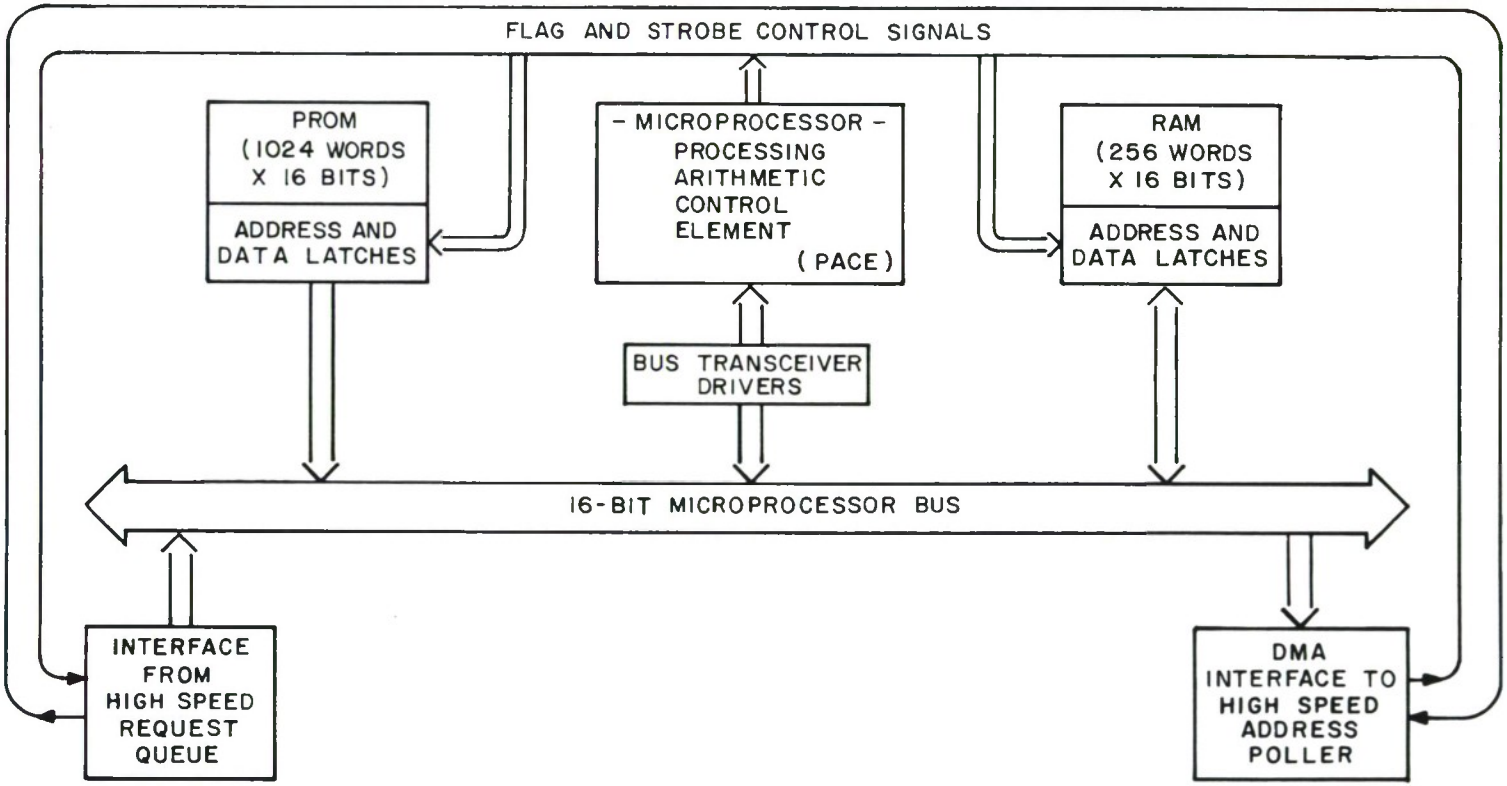

Figure 28 DATA CHANNEL CONTROLLER MICROPROCESSOR

4.3.4 Data Channel Controller Microprocessor

The Data Channel Controller uses the same type of 16-bit microprocessor as is used in the S&S Channel Controller. This provides for compatibility of design within the two controllers. As the individual designs progress, it may be determined that both functions can be handled by a single microprocessor. The microprocessor used for the MIDS laboratory evaluation configuration is manufactured by National Semiconductor Corporation and designated by the manufacturer as the Processing Arithmetic Control Element (PACE). The bus configuration for the microprocessor and its associated memory and input/output chips is illustrated in Figure 28. The microprocessor uses a 16-bit bus to provide parallel transfer of data or memory address information. The memory address information refers to the addresses used to access the contents of the Programmable Read Only Memory (PROM) and the Random Access Memory (RAM) devices. The bus multiplexes the information so that depending upon the internal microprocessor states either data or memory address information is present. The microprocessor uses flag and strobe control signals to assure proper synchronization among the various microcomputer elements connected to the bus. The input to the microprocessor is supplied by the High-Speed Request Queue, where the presence of requesting addresses are sensed by examining a "READY" bit (flag). The output from the microprocessor is supplied via direct memory access to the High-Speed Address Poller. The DMA action to reload the High Speed Poller buffer takes place every 64 polls.

The PROM storage is provided by four chips each containing 512 x 8-bits of storage configured as to provide a total of 1024 words x 16 bits. Stated another way the read-only memory capacity is 1024 words with each word containing 16 bits. The RAM storage is provided by four chips each containing 256 x 4-bits, so configured as to provide 256 words x 16 bits.

4.3.5 Microprocessor Software Programs

The microprocessor in the channel controller is used to manage the High-Speed Address Poller. The software determines which terminals are given high-speed service and how long they receive it before they are dropped back to low-speed service. The microprocessor contains two programs. The first is for initialization. It is run when the Data Channel Controller is first powered up. The initialization program clears software tables and signals the hardware to begin polling.

The second program is the principal operating program and is flow-charted in Figure 29. It is executed every 64 address polls and creates a list of 16 addresses to be polled during the high-speed address polling time slots of the following polling cycle. The hardware will interleave these 16 addresses with 16 low-speed address polls. If no explicit address assignment is made to any of the 16 polling slots, zero is assigned as a default value. The hardware will then use the same table of addresses to poll the duplex partners of these addresses interleaved with the next 16 low-speed address polls. The duplex partner addresses are formed by adding 16 to each of the table addresses. During the polling this table is contained in the hardware's High-Speed Address Poller. During each polling cycle the software is preparing a new table within the microprocessor for the next polling cycle of 64 polls. The polling cycles are illustrated in Figure 30. The polling sequence indicated in the diagram corresponds to the same polling sequence contained in Figure 21. The software timing that occurs during successive polling cycles is summarized in Figure 31. The interaction between the software and hardware during each polling cycle is described in detail in the following paragraphs.

The only output of the microprocessor is the 16-word high-speed address polling table. This table is transferred to the hardware buffer at the very end of each cycle, without any action by the program, by the use of the Direct Memory Access (DMA) hardware interface.

Requests for high-speed service are inputted to the microprocessor from the High-Speed Service Queue hardware buffer. This buffer is accessed one word at a time by the microprocessor. The buffer sets a flag to indicate that the queue contains at least one address. When an address is removed from the queue for processing by the software, either the next address enters the microprocessor or the flag is reset showing that the queue is empty. The software processes a request by putting the address in an empty word of the 16-word polling table. The address will stay in the table for approximately 29 cycles and will then be removed from the table by the software. The address and its duplex partner receive high-speed polling service as long as the address is in the table. After the address is removed, the service drops back to low speed. A new speed-up request must be made by the Subscriber Data Buffer Unit to get high-speed service again.

Requests for high speed polling are processed in the order that they are received from the High-Speed Address Request Queue. If there is no space in the High-Speed Address Table during one cycle, the address is saved for processing during the next cycle. The

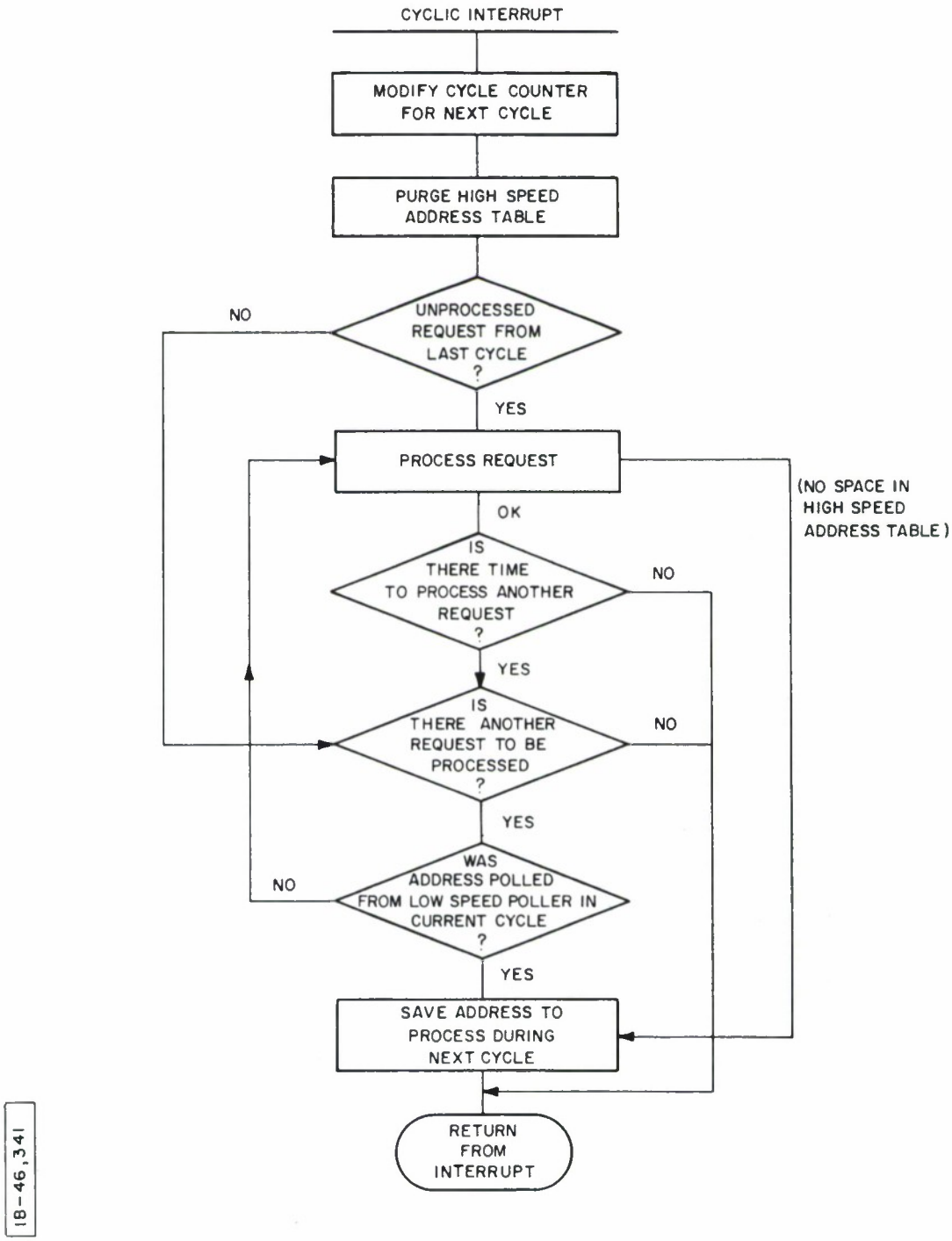

Figure 29 MICROPROCESSOR SOFTWARE FOR DATA CHANNEL CONTROLLER

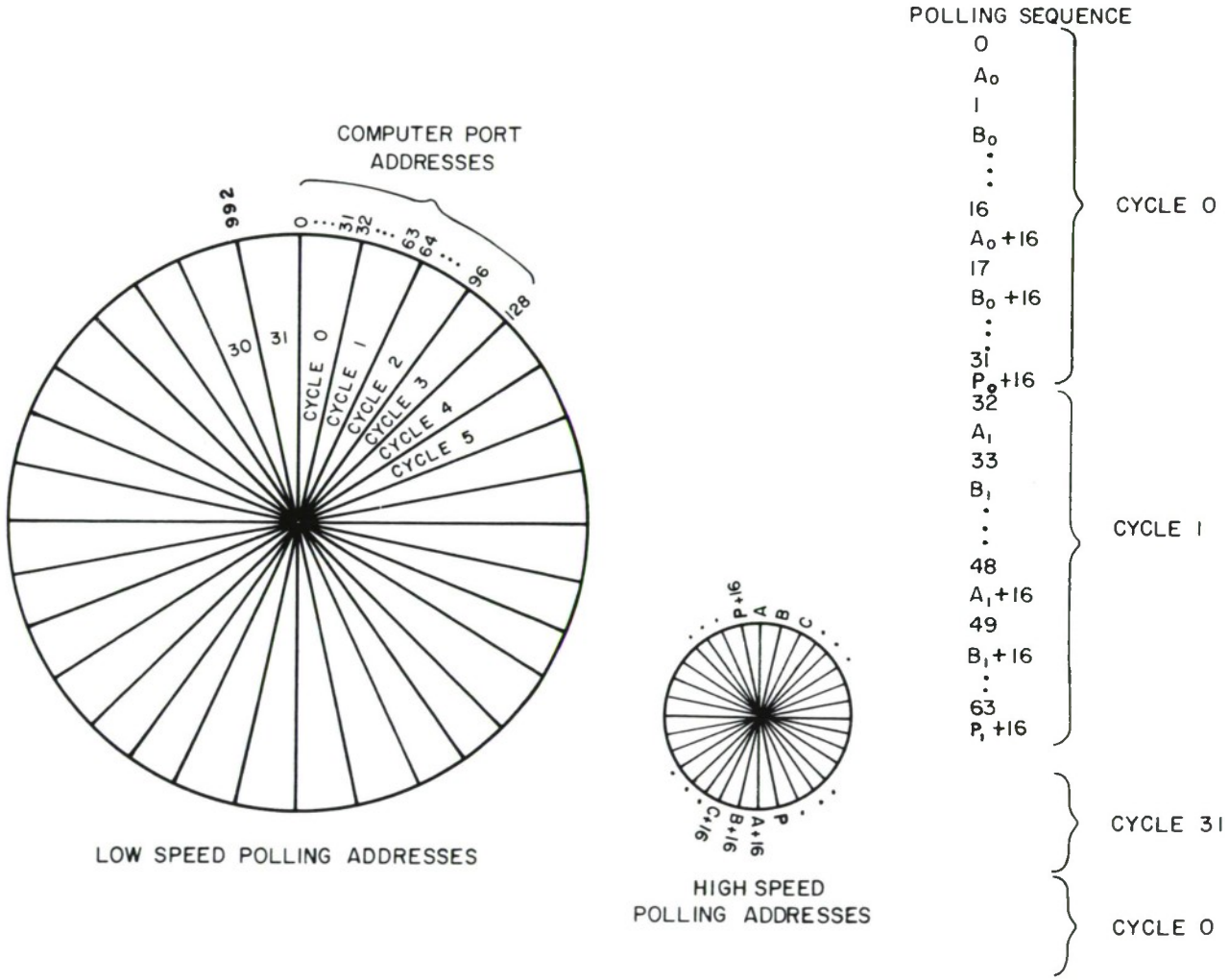

Figure 30 LOW AND HIGH SPEED POLLING SEQUENCES

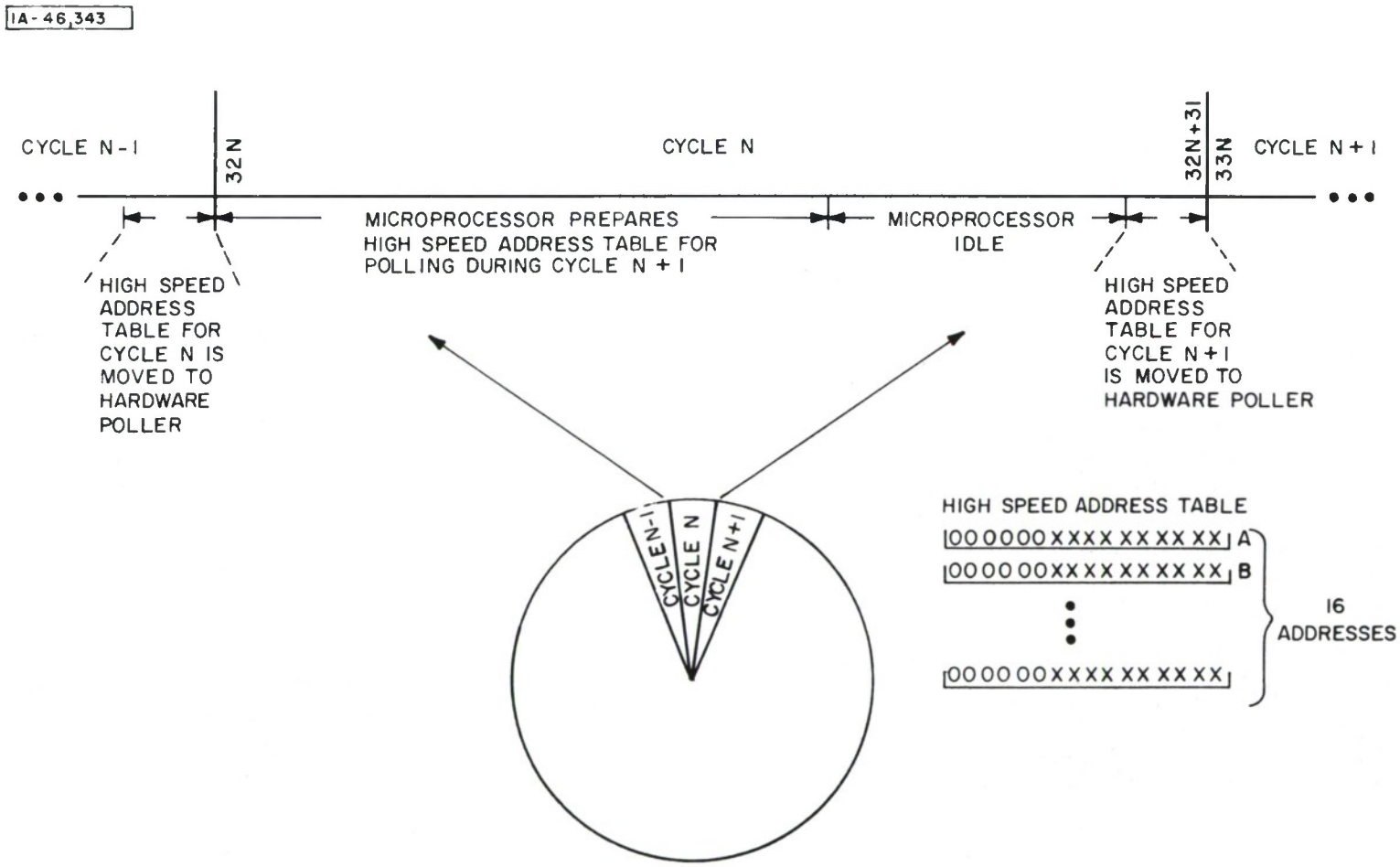

Figure 31 SOFTWARE TIMING

address will eventually get in the High-Speed Address Table. Since the amount of processing time during each cycle is limited, the software is designed to process a fixed number of high speed requests in order to be sure processing is complete before the High-Speed Address Table is turned over to the hardware for polling. Unprocessed requests are left in the request queue for the next cycle.

Each address is polled from the hardware's Low-Speed Address Poller once for every time frame whether or not the address is in the High-Speed Address Poller and whether or not an indirect address has been assigned to a terminal. There are 32 high-speed polling cycles during each time frame. Because indirect address assignments of terminals conversing with each other are made to be modulo 16, the address and its duplex partner are polled from the Low-Speed Address Poller during the same cycle. The software is designed so that an address will not be polled from the High-Speed Address Poller during the cycles immediately preceding or following its Low-Speed Address Poller cycle. This is done to assure that there will be time for a response between the polling of an address and its partner. The cycle during which an address is polled from the Low-Speed Address Poller can be determined from the five high order bits of the address. A cycle counter is maintained in the program to synchronize the software with the hardware that creates the Low-Speed Address polls. By comparing an address with the cycle counter, the software determines when the address can be assigned to the High-Speed Address Poller and when it should be taken off.

Whenever a Subscriber Data Buffer Unit is polled, it can request high speed service. The Subscriber Data Buffer Unit does not differentiate between low-speed service polls and high-speed service polls. However the request for high-speed service is recognized by the channel controller hardware only if it comes as a response to a low-speed service poll. Requests therefore are processed by the software within two or three cycles of the low-speed poll. If the request appears too soon, during the same cycle as the low-speed poll, the processing is held up until the next cycle to assure that there is one cycle without polling before the address is put in the High-Speed Address Poller. Addresses are removed from the high-speed poller by a purge of the address table at the beginning of each cycle of addresses within a certain range which is a function of the cycle counter.

4.4 SUBSCRIBER DATA BUFFER UNIT

The Subscriber Data Buffer Unit provides the interface between the subscriber's terminal and the digital data channel on the downstream and upstream cables. As part of the initial call set-up routine, an indirect transmit and receive address is sent by the S&S subsystem to the Subscriber Data Buffer Unit where these addresses are stored and compared against each message received on the downstream cable. The various functional blocks that constitute the Subscriber Data Buffer Unit are illustrated in Figure 32.

The incoming RF signals on the downstream cable are demodulated to DC level by the data demodulator portion of the modem. The Data Demodulator supplies message sync bits, clock bits, and data information bits to the logic circuits within the Indirect Address Comparator block. The data information bits are also supplied to the Receiving Register. The Indirect Address Comparator checks the polling address field to determine if the indirect transmit address received previously from the S&S subsystem matches the polling field. If a match is found, a signal is sent to the transmitting register to begin transmitting on the upstream cable. The Indirect Address Comparator then checks the next message field, that is the control and address field. It determines whether the indirect receiver address matches the receiver address in the message. If a match is found, a signal is sent to the Receiving Register to start receiving. Upon receipt of the signal, the Receiving Register accepts the next four data words in bit-serial mode and then transfers them in bit-parallel mode to the microprocessor. The microprocessor in turn transfers the data information via the logic circuits within the Terminal Interface block to the subscriber's terminal unit.

The microprocessor manages the data flow between the subscriber terminal and the MIDS digital data channel. The microprocessor monitors the quantity of data within its buffer to determine if the subscriber's terminal needs high speed service. If a threshold level within the buffer is exceeded, the microprocessor sets the high-speed request bit in the control field of the message to be transmitted. The microprocessor also indicates to the destination terminal whether the message being sent is an original transmission or a retransmission.

When the Subscriber Data Buffer Unit is receiving messages, the microprocessor requests a retransmission if the Receiving Register detects bad parity within an incoming message. Request for retransmission is also used to provide data rate smoothing, i.e., to effect a hold up of data transmission. If a terminal is unable to

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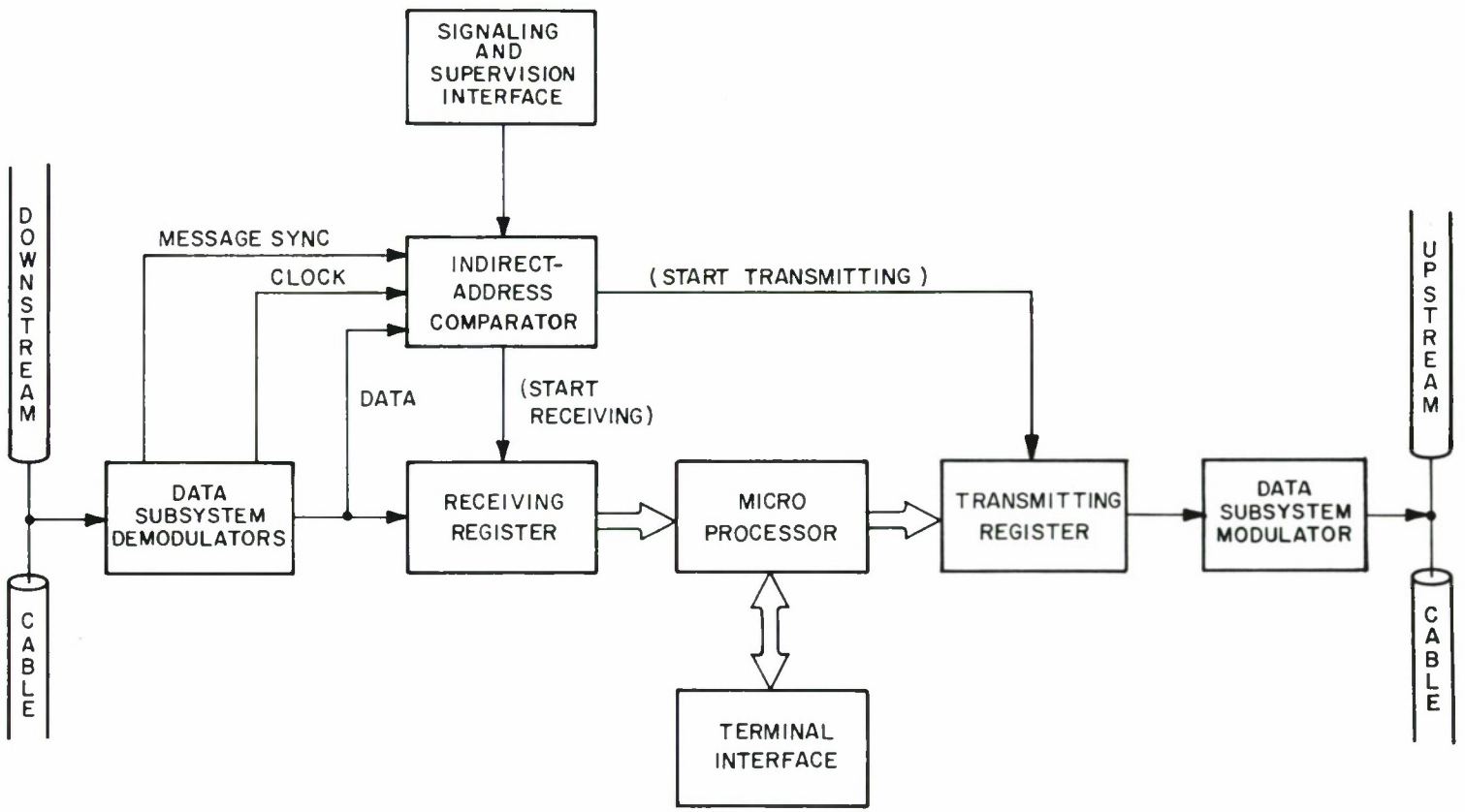

Figure 32 SUBSCRIBER DATA BUFFER UNIT

accept new data for any reason, it requests a retransmission. The retransmitted data is then noted by the receiving microprocessor and ignored. If the receiving terminal is still unable to accept new data, it again requests retransmission. Again no new data is sent, only a repeat of the last message, and again it is ignored. The timing of the request to retransmit always takes place 32 polling times after the message was received. Each sending terminal buffers the old message for that time period to insure that it is available for retransmission.

The flexibility of the microprocessor software is also used to compensate for different character codes, etc., so that customized hardware interfaces between the Subscriber Data Buffer Unit and different types of subscriber terminal devices is not required.

4.5 MULTIPORT DATA BUFFER UNIT

In order to provide simultaneous multiple terminal access to common-user facilities such as a data processing computer, a multiport data buffer unit is advantageous. The multiport data buffer unit being developed is capable of providing communication between 64 terminals on the cable and a large host-processor computer. The host processor would interface to the buffer through a front-end-processor such as a PDP 11-40 minicomputer. The reason for using the multiport data buffer unit rather than a set of individual subscriber data buffer units is that common circuits may be used. For example, only one set of modems is required by the buffer unit to interface the cable. Thus, the many-to-one connectivity of multiple terminals to a host computer is economically achievable. The multiport data buffer is being developed under Project 902C as a MITRE IR&D Task.

For the MIDS laboratory evaluation the Multimode Data Buffer system will provide multi-terminal access to an IBM 370/158 time-sharing computer. A Programmed Front-End-Processor is used to emulate an IBM 2703 Transmission Control Unit and interfaces the Buffer Unit to the IBM 370/158. The interconnections between the Programmed Front-End-Processor, the Buffer Unit, and the upstream and downstream cables are indicated in Figure 33.

The present design for a Multiport Data Buffer Unit contains 64 registers for control words that are built during the call set up by the Signaling and Supervision Subsystem. In association with each control word an address register is provided which will contain and identify the indirect receiving address of incoming data messages. The control word register itself also contains characteristics of

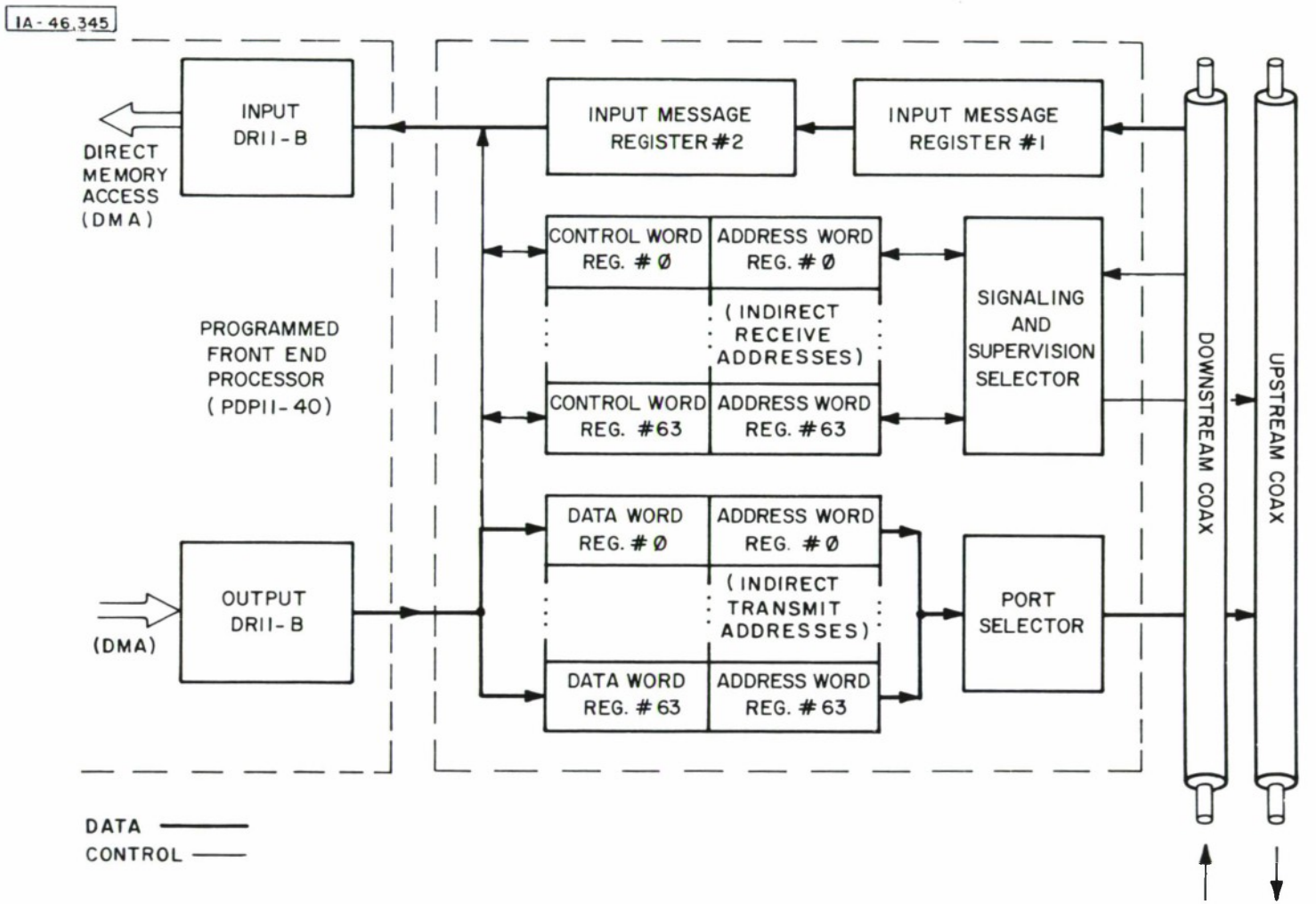

Figure 33 MULTIPORT DATA BUFFER

the subscriber terminal device that is requesting a time-shared connection. These characteristics include such information as the subscriber terminal's data rate, type of code and format(e.g., ASCII or EBCDIC) The information stored in the control word and associated address word register is transferred to the Front-End-Processor as part of the initial call set up routine. It should be noted that the 10-bit address word is not transferred to the front-end-processor but only the seven low-order bits which define a block of 128 addresses. The Digital Data Channel Controller reserves the first 128 addresses in the sequence of 1024 addresses for the Multiport Data Buffer Unit.

When an incoming data message is recognized on the downstream cable, the Multiport Data Buffer circuits examine the address in the message to see if it matches any of the addresses in the bank of receiving addresses. If a match is found, the data information portion of the message is stored in Input Message Register #1. The register's contents are then transferred bit parallel to Input Message Register #2. The use of the double buffer arrangement frees Input Message Register #1 for accepting in bit-serial mode another message from the downstream cable.

When a data message is subsequently received, only the access port address and the actual data portion of the message is transferred to the front-end-processor. The transfer control process is via a direct memory access. The single direct memory access (DMA) transfer of the address word and the four data words is faster than a succession of five normal transfers. The direct memory access procedure is used to assure that the content of Input Message Register #2 is forced into memory so that the Multiport Data Buffer Unit will not cause a "backup" on the downstream cable.

Messages from the host processor to be transmitted on the upstream cable are received by the Multiport Data Buffer Unit from the Front-End-Processor. A direct memory access feature is also used in the upstream direction. The Multiport Data Buffer Unit contains a bank of holding registers to handle the upstream coaxial cable messages. This bank of registers includes 64 data word registers and their associated indirect transmit (upstream) address word registers. The data word registers contain the actual data information in four 16-bit words. The address word registers contain the indirect transmit address assigned by the Front-End-Processor, and related to the receiving address by adding 16. The Port Selector circuit is activated after detection of the polling address on the downstream cable. The Port Selector accesses the corresponding Data Word register and causes the words to be read out onto the upstream coaxial cable.

The Multiport Data Buffer Unit diagram in Figure 33 emphasizes information flow between the cables and the communications Front-End-Processor. For the sake of diagram simplicity the S&S subsystem modem and the Digital Data subsystem modem were omitted. In actual practice one of each type modem would be used with the Multiport Data Buffer Unit as indicated in Figure 1.

4.6 DATA DISTRIBUTION SUBSYSTEM MODEM

The Data Distribution Subsystem Modem provides the coaxial cable interface for the data distribution subsystem's channel controller, subscriber data buffer units and the multiport data buffer unit. As described in Sections 4.1 and 4.2 the Data Distribution Subsystem total data transmission rate is 2.25 megabits per second on a 13.5 megaHertz carrier with a message block length of 104 bits.

Data systems must deal with the three transmission and detection problems of data, clock and message synchronization. Effective data transmission requires that data sampling by the receiver be accomplished at the right time and proceed at the proper rate. In data communication systems that are to handle many different users the modems should be simple and low cost. Data modems that use elaborate data-encoding techniques or expensive timing sources need to be avoided. Therefore, a data modem that uses a unique tri-phase modulation technique is being developed for MIDS that permits simple encoding and detecting of data, clock and message synchronization over one differential phase-shift-keyed transmission channel. A simplified block diagram of the major components of the tri-phase modem is shown in Figure 34.

In the modem a stable reference frequency is obtained from a crystal-controlled oscillator stage operating at 13.5 megaHertz. An "on/off" control line is provided to an output amplifier associated with the oscillator circuit so that the modem is only on-line while it is actually transmitting a message block. The output of the oscillator stage is applied to a phase-splitter network. The phase-splitter network provides three 13.5 megahertz signals each separated in phase by 120 degrees. The signals at 0 degrees and 120 degrees are supplied to a gate controlled, two-channel-input, wideband amplifier. The output of this circuit and the third Phase-Splitter output at 240 degrees are applied to a second gated amplifier circuit. The output of the final amplifier stage is applied to the coaxial-cable line at a level of 200 millivolts rms (46 dbmv). The control lines for switching the proper phase to the coaxial cable are provided by a 3 State Up/Down Counter.

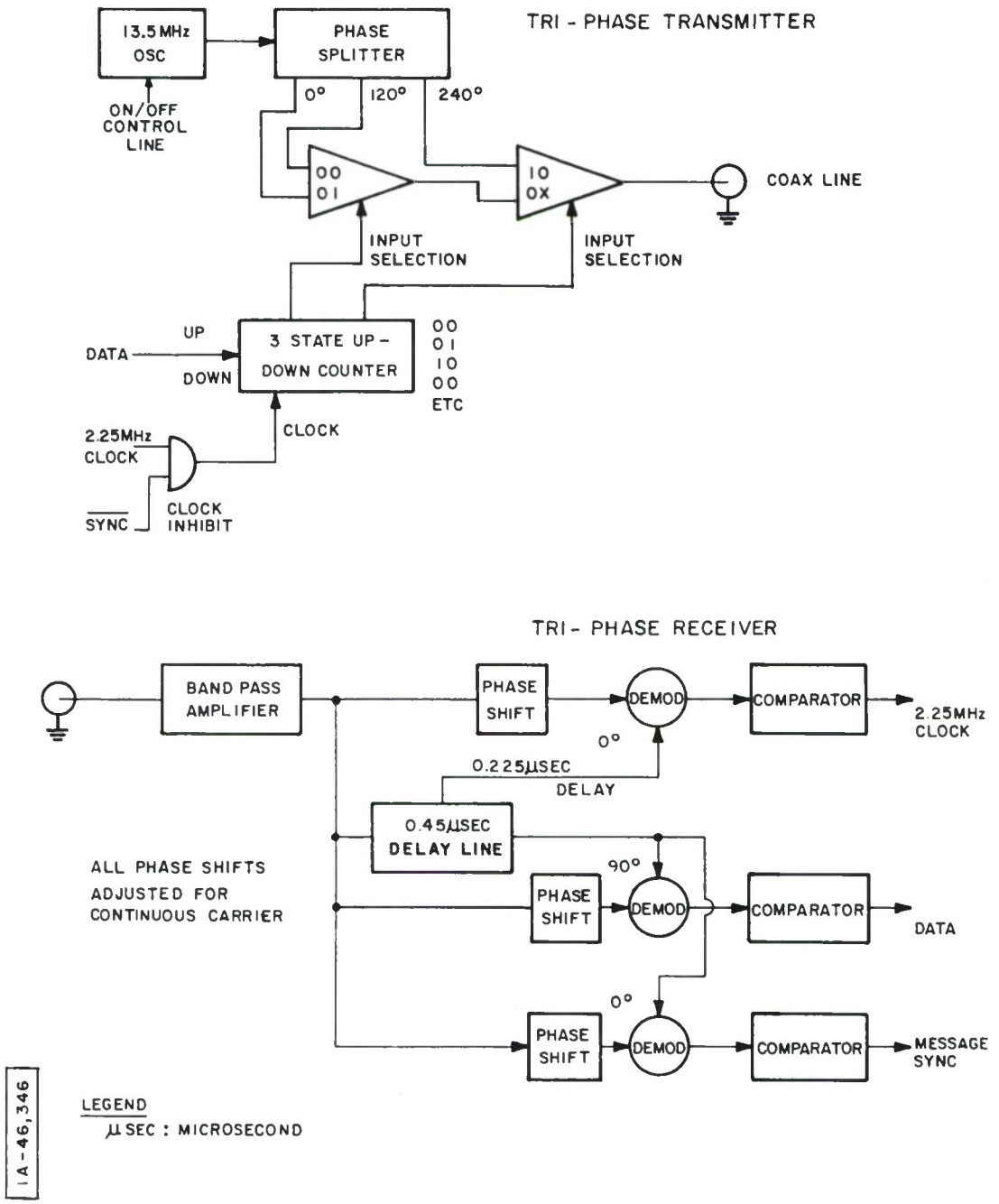

Figure 34 DIGITAL DATA SUBSYSTEM MODEM

At the beginning of each message block three message synchronization periods are sent by the modulator. During the synchronization period the 2.25 megaHertz clock is inhibited from driving the counter. As a result the phase of the 13.5 megaHertz frequency remains the same on the coaxial cable line. When the Message-sync periods are complete, the sending tri-phase transmitter's AND gate is enabled and a 2.25 megaHertz clock is then applied to the Up/Down Counter. The data from the sending source is applied to the common "up/down" line of the counter. A stream of continuous 1's from the data source causes the phase shifts to rotate in a counter clockwise direction, for example, 0 degrees to 120 degrees for the first 1, 120 degrees to 240 degrees for the second 1, etc. A stream of continuous 0's will cause the phase to rotate in the opposite direction. A random stream of 0's and 1's will vary the phase shift in direction in accordance with whether the bit changes from 0 to 1 or 1 to 0. In summary the significant point is that a phase shift always occurs from one bit time to the next.

The tri-phase receiver of the receiving terminal's modem is capable of accepting incoming signals in the range from 1 to 10 millivolts rms (0 to 20 dbmv). The signals are passed through a bandpass amplifier circuit and then to three separate phase-shifting circuits. As part of the initial system line-up procedure, the channel controller modem sends a continuous, unmodulated carrier and the Phase Shift circuit in the Data Demodulator stage is adjusted to produce 90 degrees as indicated in the diagram. The phase shift circuits in the other two demodulator stages are adjusted to produce zero degrees between the two inputs to each demodulator.

The three demodulators operate on a vector multiplication principle such that if the two incoming signals to the demodulator are less than 90 degrees apart, a positive output is produced. If the two signals are more than 90 degrees apart, then a negative output is produced. This is the basis of the three-phase encoding/decoding technique.

At the receiving terminal a Data Demodulator correlates the phase of the signal being received to the phase of the signal received on the previous transmission. After the incoming signal is passed through the 90 degree Phase Shift stage, the phase difference between the two signals is applied to the demodulator. There are only two choices of resulting phase shifts. For example, the subtraction of 90 degrees from 120 degrees or 240 degrees due to the Phase Shift circuit leaves either 30 degrees or 150 degrees respectively. Therefore, the Data Demodulator operates on input signals that are either 30 degrees or 150 degrees apart. The

difference in polarity of these signals is strong enough to provide accurate driving of the demodulator. If the Data Demodulator detects a phase difference of 30 degrees, it sends a "positive-going" signal to the Comparator. If it detects 150 degrees, it sends a negative-going signal to the Comparator. The Comparator circuit squares-up and smooths the voltage wave shape so that the logic circuits of the external interface may be driven by the appropriate dc-level signals.

A second demodulator is used to obtain a clock frequency. It should be noted that the delay line used for the Data Demodulator operates over a full bit-time period, that is six sine-wave cycles, and also contains a half-period delay tap. The Clock Demodulator correlates the selected signal against each prior signal for the first half-period and then against the selected signal itself for the second half-period. The vector products will first be a negative signal and after the half-period delay, a positive signal. The result is a square-wave output from the Comparator circuit at the highest data bit rate. The clock signal is supplied to the external logic circuits for clocking the incoming data bits.

A third demodulator is used to obtain message block synchronization. During the message synchronization period the transmitting terminals' modem does not shift the phase of the carrier signal for three successive periods. As a result the message synchronization demodulator correlates identical signals during the second and third time periods and produces two positive output signals. After shaping by the Comparator circuit, these two signals are used by the Subscriber Data Buffer Unit as an indication of the start of the message block.

SECTION V

IMPLEMENTATION

During FY 76 the design and fabrication of the system and subsystem elements described in the previous sections will be completed. These elements will then be assembled into a MIDS configuration and connected to the MITRE in-house coaxial cables. The Multiport Data Buffer Unit, developed under separate MITRE IR&D funds, will also be completed and available in FY 76. It will be connected to the coaxial cables and the MITRE IBM 370/158 computer to permit complete testing of the MIDS configuration.

Tests will be conducted to determine hardware and software performance, system traffic loading acceptability and ease of use by the subscribers. The ability of the MIDS S&S and Data Distribution subsystems to operate without interference from other services on the cable will be evaluated. It is also equally important to ascertain that the MIDS subsystems do not affect the other services. For this reason the testing effort will be formally divided into susceptability tests and emission tests.

Operational traffic testing is also planned. A number of IBM typewriter terminals and visual display terminals will access the IBM 370 computer through use of the Multiport Data Buffer Unit. System response time and the performance of the automatic adaptive data rate feature will be monitored. The test results will be used to finalize system concepts and design approaches.

APPENDIX A

ADAPTIVE DATA RATE TRAFFIC ANALYSIS

Introduction

This analysis explains the dynamic relationship between the buffer within the Subscriber Data Buffer Unit (SDBU) and the pollers in the Channel Controller. The ability of the Data Distribution Subsystem to appear transparent to a large number of terminals with different transmission rates is derived. This automatic adaptive data rate feature is most easily described by a typical example. One such example would involve data transfer between visual display terminals and a host computer.

As a starting point in the analysis it is assumed that the visual display terminals have the following characteristics:

- o transmit at data rate of 9600 bps
- o contain local storage for 2,000 characters
- o use a 10-bit ASCII code

These are characteristics common to many commercial visual display terminals.

Certain simplifying assumptions regarding the system are made to more effectively highlight the principles of the adaptive data rate feature. The assumptions used in this example are as follows:

- o Low speed polls occur at a rate of 10 per second, rather than 10.34.
- o High speed request messages are immediately serviced, rather than potentially queued.
- o A full 32 polls occur, including low-speed and high-speed polls, during the emptying cycle of the buffer, rather than 30.

Mechanics of Low-Speed and High-Speed Polling

The filling-up and emptying of the microprocessor storage area, hereafter called the buffer, is illustrated in Figure A-1.

The subscriber's terminal may start transmitting at any time between polls. The reception of the low-speed polls is shown in

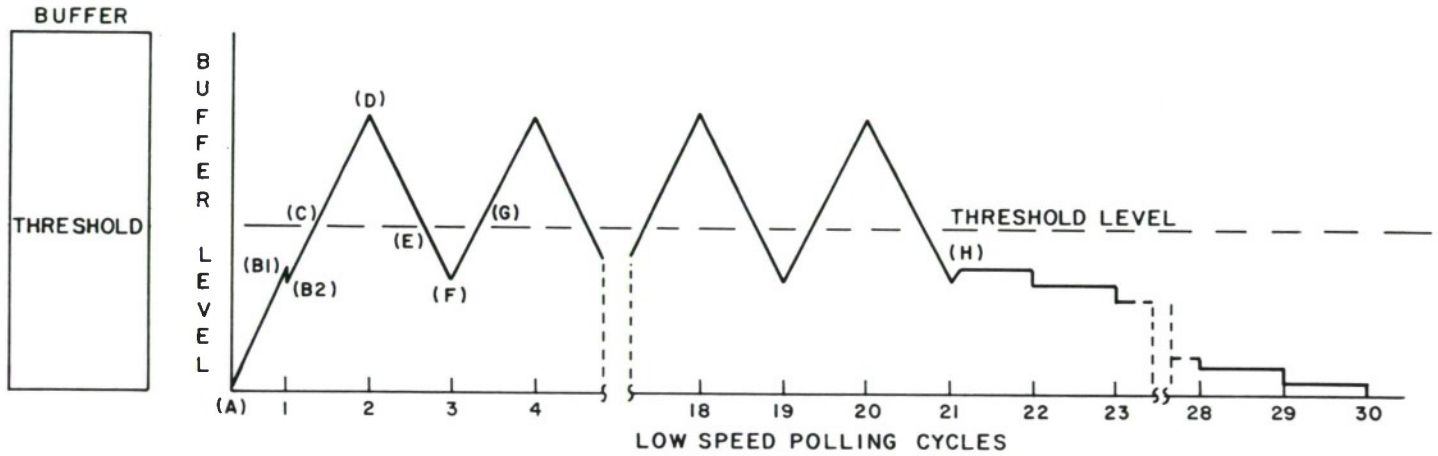

Figure A-1 ADAPTIVE DATA RATE BUFFER

the diagram at 1, 2, 3, etc. The start of transmission of the subscriber's terminal is arbitrarily chosen and is indicated by the point (A). As the subscriber's terminal transmits, the buffer starts to fill up. When the Subscriber Data Buffer Unit receives the first low-speed poll, the buffer has filled up to the level indicated by (B1). Upon receipt of the poll the Subscriber Data Buffer unit sends 8 characters as indicated by (B2). Since the subscriber's terminal is still transmitting, the buffer continues to fill up. When the threshold level is reached at point (C), a high-speed request bit is set. The buffer continues to accept data until the second low-speed poll is received. At this point (D) the subscriber data buffer unit sends the high-speed request bit. It is assumed that the Subscriber Data Buffer Unit is assigned immediately to the high-speed poller by the channel controller. The buffer starts emptying in response to the succession of high-speed polls. At point (E) the buffer has dropped below the threshold level and the high-speed request bit is cleared. The buffer continues sending in response to the high-speed polls. At point (F), the Subscriber Data Buffer Unit receives the third low-speed poll. However, a high-speed request bit is not sent to the Channel Controller. The Channel Controller in turn discontinues sending high-speed polls to that subscriber data buffer unit. The buffer therefore starts to fill up again and at point (G) the threshold is reached and the high-speed request bit is set.

The buffer continues to fill-up and empty in accordance with the mechanics just described. Upon receiving the 21st low-speed poll the buffer receives only 8 additional characters from the subscriber's terminal. At this point (H) the subscriber's terminal has completed its transmission of 2000 characters. However, the Subscriber Data Buffer unit still has 72 characters in storage. The buffer never reaches the threshold level again and empties at each succeeding low-speed poll by 8 characters. Upon reception of the 30th low-speed poll the buffer has been completely emptied. Of course other subscriber data buffer units are using the high speed poller during this "trailing" period.

In summary the buffer only requests high-speed service when it can respond with data to all the high-speed polls that will occur between the next two low-speed polls. This characteristic of the adaptive data rate design is the key to the efficient use of the data channel by a large number of subscriber terminals.

Buffer Size and Operation

As indicated in Figure A-1 the subscriber's terminal may start transmitting at any point in time between the low-speed polls.

Under worst case conditions the terminal may start transmitting just after a low-speed poll is received by the SDBU. Therefore the buffer should be capable of storing data transmitted by the terminal during two successive low-speed polling intervals.

A terminal transmitting at 9600 bps using 10-bit ASCII character encoding is equivalent to transmitting 960 characters per second. (The 10-bit character includes Start, Stop, Parity and 7 Information bits.) Since a low-speed polling cycle is approximately 0.1 seconds in duration, 96 characters are transmitted each cycle. The buffer storage requirement is 2 x 96 or 192 characters.

The threshold level of the buffer should be set at the 96-character storage point. When this point is reached, the Subscriber Data Buffer Unit will set the high-speed request bit in its control message. The control message will be sent upon the receipt of the next low-speed poll. Under the worst case conditions the buffer will then be at the 186 character storage point. Since instantaneous access to the high-speed poller is assumed, the buffer will start to output on the cable simultaneously with the transmission of the terminal device itself. It should be noted that the "line" speed of the coaxial cable is 19.2 kilobits per second for each temporarily-assigned, high-speed terminal. If the terminal device is sending at 9600 bits per second, the buffer provides the difference in the transmission rate. In other words, the buffer is effectively outputting at 9600 bits per second. In summary, the buffer receives and stores data from the terminal device between low-speed polls and it pumps data onto the line during the high-speed polling cycle.

The significant area within the buffer is the zone containing the 96 characters stored between the receipt of two low-speed polling cycles e.g. (B2) and (D) of Figure A-1. This zone physically varies within the buffer depending upon the relationship between the start of transmission of the terminal device and the occurrence of the terminals' low-speed poll in the polling cycle. Once the buffer is being serviced by the high-speed poller, the zone empties enough during the high-speed cycle so that it drops below the threshold level and the high-speed request is not sent upon completion of the next low-speed polling cycle. Therefore, the buffer becomes a receiver of data from the transmitting terminal during the next low-speed polling cycle time. Upon the completion of that time period the threshold level is reached and the high-speed request bit is set so that the next low-speed polling cycle in effect becomes the start of the high-speed cycle. In summary for a subscriber's terminal transmitting at 9600 bps and after the initial partial low-speed polling cycle, the buffer receives during the

first full-time low-speed polling cycle, transmits during the second, receives during the third, transmits during the fourth, etc.

For the case of a 4800 bps terminal, the buffer will accept data from the terminal for three successive low-speed polling time periods and transmit on the cable during the fourth, receive for the next three cycles and transmit during the fourth, etc. In effect, the automatic adaptiveness of the system has caused the system to appear transparent to the terminal. The system can simultaneously service 16 pairs of terminals operating at 19.2 kilobits, 32 pairs of terminals operating at 9600 bits per second, etc., as indicated in the following tabulation.

Pairs of terminals	Terminal data rate
16	19,200 bps
32	9,600 bps
64	4,800 bps
128	2,400 bps
256	1,200 bps

Regarding the pairs of terminals, the other half of the pair may be a computer. In addition to the above listing the system can still service simultaneously the remaining terminals at the standard 600 bps rate.

Traffic Example

An important type of traffic being offered to visual display terminals is in the area of word processing or text editing. The use of the terminal for textual material includes both entering the text and then later editing the text. For purposes of this analysis it is estimated that it takes approximately two minutes to enter a screen of text. In the subsequent editing mode it is estimated that the text can be edited at a rate of 7 to 8 screens per minute. With many operators using the terminals, on the average, there will be a mixed mode of entering and editing. It is estimated that 1/3 of the operators will be entering original text and 2/3 of the operators will be editing text during any given time interval. A busy hour analysis for each of these modes is described.

In the entering mode the average terminal will be requesting high-speed service once every 2 minutes, that is 30 times an hour. From the preceding diagram on the mechanics of the high-speed and low-speed poller it was indicated that ten high-speed polling periods will accommodate a 2,000 character message. Each of these polling periods lasts for one tenth of a second. The total amount

of time in the high-speed poller is one second per message. Therefore the terminals use the high-speed poller for 30 seconds during each busy hour. The probability of usage for a single terminal is P = 30/3600 = 0.0083. Assuming 512 terminals with a similar duty cycle means that on the average there will be 512 x 0.0083 = 4.3 terminals entering text simultaneously. The binomial standard deviation of this number is 2.05. Thus the majority of fluctuations from the average lie in the range of 2 to 6 pairs of terminals. Since the system can accommodate 32 pairs of terminals operating at 9600 bits per second simultaneously, all terminals operating in the entering mode do not present a congestion problem.

In the editing mode the usage of the high-speed poller goes up significantly. A single terminal requesting the high-speed poller at a rate of eight times a minute is equivalent to sending 480 messages per hour. The probability of usage is P = 480 x 1 sec/3600 = 0.075. If all 512 terminals were using the editing mode, the average number of simultaneous requests equals 38.4. The standard deviation is approximately 6. Therefore the majority of fluctuations will range from 32 to 44. With only 32 pairs of "spaces" available in the high-speed poller, there will be contention in the system. However the system is non-blocking in the sense that the system will slow down before it blocks any of the 512 terminals. This occurs because the users already transmitting in the high-speed mode are not given preference over users requesting high-speed service. Therefore the apparent transmission speed decreases in accordance with the number of users simultaneously requesting high-speed service. Using the "worst case" upper value of 44 the effective throughput will be equal to 32/44ths x 9600 bits per second or 7,000 bits per second. In other words the system has a graceful degradation characteristic rather than a blocking characteristic.

In the mixed mode, whereby some operators are entering text and others are editing text, the probability of usage falls between the two extremes analyzed above. If a single terminal is entering text one third of the time and editing text two thirds of the time the probability of usage is P = 1/3 x 0.0083 + 2/3 x 0.075 = 0.0528. The average number of simultaneous requests from 512 terminals is 27.03 with a standard deviation of approximately 5. Therefore the likely fluctuation from the normal will be between 22 and 32 terminals simultaneously in use. Since the system can accomodate 32 terminals simultaneously, the mixed mode presents no potential congestion and all 512 terminals can operate at their full data speeds of 9600 bits per second.

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4. INTEL Corporation, MCS-40 User's Manual for Logic Designers, Santa Clara, California, March 1975.

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DEPARTMENT OF THE AIR FORCE
HEADQUARTERS ELECTRONIC SYSTEMS DIVISION (AFSC)
HANSCOM AIR FORCE BASE, MASSACHUSETTS 01731

REPLY TO
ATTN OF: DRI

20 January 1976

SUBJECT: **ESD-TR-75-303, MIDS Network Control and Digital Data Subsystem Designs, December 1975**

TO: DDC/Air Force Liaison Representative
Andrews AFB, Washington, D.C.

1. I certify that the subject TR has been reviewed and approved for public release by the controlling office and the information office in accordance with AFR 80-45/AFSC Sup I. It may be made available or sold to the general public and foreign nationals.

2. Distribution statement A appears on the subject TR and the DD Form 1473 as required by AFRs 80-44 and 80-45.

FOR THE COMMANDER

original signed by
E. M. Doherty
EDWARD M. DOHERTY
Chief, Scientific & Technical
Information Division

1 Atch
ESD-TR- 75-303
(12 cys)

THE MITRE CORPORATION

BEDFORD, MASSACHUSETTS

13 January 1976 C18-16

Commander
Electronic Systems Division
Air Force Systems Command
L. G. Hanscom Field
Bedford, Massachusetts 01731

Attention: E. M. Doherty, DRI

Subject: ESD-TR-75-303 (MTR-3061)

Gentlemen:

We are enclosing 42 copies of ESD-TR- 75-303 , 2 for DDC, two for your files and one for the Air Force University. Publication and distribution of this document have been mutually agreed upon by MITRE and ESD project personnel.

Sincerely,

Claire G. Bentley
Publications

Attachments (42)

/cgb

DEPARTMENT OF THE AIR FORCE
HEADQUARTERS ELECTRONIC SYSTEMS DIVISION (AFSC)
LAURENCE G. HANSCOM FIELD, BEDFORD, MASSACHUSETTS 01730

REPLY TO ATTN OF: DRI (Mrs. Bryer/2926/S 22) 22 October 1975

SUBJECT: Transmittal of Approved ESD/MITRE Technical Report

TO: The MITRE Corporation
Technical Publications
Attn: C. Bentley, Dept. A410

The attached report has been reviewed and approved by the project officer as an ESD Technical Report. The proper approval statement and release notices for the report are **18, 20, and Statement A. Please include attached introductory narrative included by the Project Office. Please include the Project Office (XRE) for ten (10) copies of the completed report. Copies to OIP are no longer required.**

EDWARD M. DOHERTY
Chief, Scientific & Technical
Information Division

3 Atch
1. **Introductory Material**
2. **Review and Approval**
3. **ESD-TR-75-303 (MTR-3061)**

DEPARTMENT OF THE AIR FORCE
HEADQUARTERS 3245TH AIR BASE GROUP (AFSC)
HANSCOM AIR FORCE BASE, MASSACHUSETTS 01731

REPLY TO ATTN OF: OIP/5322/S 27

20 October 1975

SUBJECT: Review of Technical Document

TO: DRRI

Identification: ESD-TR-75-303 (MTR-3061)

OIP has no objection to release of the above-cited document to the National Technical Information Service (NTIS).

JOHN T. O'BRIEN
Chief, Public Information Division
Information Office

1 Atch
ESD-TR-75-303 (MTR-3061)

DEPARTMENT OF THE AIR FORCE
HEADQUARTERS ELECTRONIC SYSTEMS DIVISION (AFSC)
LAURENCE G. HANSCOM FIELD, BEDFORD, MASSACHUSETTS 01730

REPLY TO ATTN OF: DRI (Mrs. Bryer/2926/S 22) 16 October 1975

SUBJECT: Release of Documents to the National Technical Information Service (NTIS)

TO: OIP (Mr. J. O'Brien)

Please review the attached document, ESD-TR-75-303 (MTR-3061)

for release to the National Technical Information Service (NTIS).

EDWARD M. DOHERTY
Chief, Scientific & Technical
Information Division

1 Atch
ESD-TR-75-303

DEPARTMENT OF THE AIR FORCE
HEADQUARTERS ELECTRONIC SYSTEMS DIVISION (AFSC)
HANSCOM AIR FORCE BASE, MASSACHUSETTS 01730

REPLY TO ATTN OF: DRI (Ms. Bryer/2926/S 22) 19 September 1975

SUBJECT: Proposed ESD Technical Report (MTR-3061, MIDS Network Control and Digital Data Subsystem Designs)

TO: XRE (Mr. Westley)

1. The attached MITRE Report is forwarded for your approval or disapproval as an ESD Technical Report. Request your review within ten (10) working days of the date of this letter.

2. If you approve this report for publication as an ESD TR, complete the following:

a. Examine the report for technical competence and proper security classification. Choose either distribution Statement A or B, from the attached abstracted AFR 80-45 (attachment 1). (NOTE: Classified documents do not require a distribution statement unless the project officer feels that one would insure distribution limitation in addition to "need-to-know" requirements imposed by AFR 205-1, or in the event the document is declassified. In such an instance, Statement B. with the proper reason may be used.)

b. Enter your distribution statement choice on the ESD Form 33 (attachment 2), and sign it. The remainder of the form will be completed by this office.

c. Prepare a Review and Approval Statement using attachment 3 as a guide. (Please be sure your signature does not touch the typed signature element.)

d. Return the entire package (the Review and Approval, the ESD Form 33, and the MTR) to XRRI for final processing. Please note the number of copies your office will require of the completed ESD TR.

e. Inform XRRI of the proper security markings for classified reports.

3. If you decide this report should not be published as an ESD TR, inform this office in writing.

EDWARD M. DOHERTY
Chief, Scientific & Technical
Information Division

4 Atchs
1. Abstracted AFR 80-45
2. ESD Form 33
3. Sample Review and Approval
4. MTR-3061

THE MITRE CORPORATION

BEDFORD, MASSACHUSETTS

17 September 1975 C34-2157

Commander
Electronic Systems Division
Air Force Systems Command
Hanscom Air Force Base
Bedford, Massachusetts 01731

Attention: E. M. Doherty, DRI

Subject: ESD-TR Candidates (MTR-3050; MTR-3061; MTR-3080; MTR-3087)

Gentlemen:

The attached MITRE reports are forwarded as ESD-TR candidates.

Sincerely,

Claire G. Bentley

Claire G. Bentley
Publications

Attachments
MTR-3050 "Use of a FORTRAN Frequency Analyzer to Develop Synthetic FORTRAN Programs"
MTR-3061 "MIDS Network Control and Digital Data Subsystem Designs"
MTR-3080 "Software Acquisition Management Guidebook: Regulations, Specifications and Standards" RUSH - per telecon Capt Wkte. MCI
MTR-3087 "Computer Network Engineering Plan"

/cgb